REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE:

SDM636 GPIO Configuration For Starlord

GPIO_0	DBM_UART0_RXD	GPIO_42	ID0	GPIO_84	UIM2_CLK
GPIO_1	DBM_UART0_TXD	GPIO_43	ID1	GPIO_85	UIM2_RESET
GPIO_2	I2C_TP_SDA	GPIO_44	ID2	GPIO_86	UIM2_PRESENT
GPIO_3	I2C_TP_SCL	GPIO_45	REAR_CAM_AVDD1V8_EN_2	GPIO_87	UIM1_DATA
GPIO_4	TEST_TX	GPIO_46	REAR_CAM_DVDD_EN_2	GPIO_88	UIM1_CLK
GPIO_5	TEST_RX	GPIO_47	CAM1_RST_N	GPIO_89	UIM1_RESET
GPIO_6	BLSP2_I2C_SDA	GPIO_48	CAM2_RST_N	GPIO_90	UIM1_PRESENT
GPIO_7	BLSP2_I2C_SCL	GPIO_49	LDM_IDO	GPIO_91	UIM_BATT_ALARM
GPIO_8	BLSP_SPI3_MOSI	GPIO_50	CAM_AF_VDD_EN	GPIO_92	DRX_TUNER_SW0
GPIO_9	BLSP_SPI3_MISO	GPIO_51	CAM_AVDD_EN	GPIO_93	DRX_TUNER_SW1
GPIO_10	BLSP_SPI3_CS_N	GPIO_52	CAM3_RST_N	GPIO_94	DRX_TUNER_SW2
GPIO_11	BLSP_SPI3_CLK	GPIO_53	LCD_RESET	GPIO_95	DRX_TUNER_SW3
GPIO_12	AUDIO_MI2S_SCK	GPIO_54	NC	GPIO_96	DRX_TUNER_SW4
GPIO_13	AUDIO_MI2S_WS	GPIO_55	LDM_ID1	GPIO_97	DRX_TUNER_SW5
GPIO_14	AUDIO_MI2S_D0	GPIO_56	NC	GPIO_98	PRX_TUNER_SW4
GPIO_15	AUDIO_MI2S_D1	GPIO_57	FORCED_USB_BOOT	GPIO_99	QLINK_REQUEST
GPIO_16	RXD	GPIO_58	USB_PHY_PS	GPIO_100	QLINK_ENABLE
GPIO_17	TXD	GPIO_59	LCD_TE	GPIO_101	RFFE1_DATA - WTR6955 debug
GPIO_18	RTS	GPIO_60	NC	GPIO_102	RFFE1_CLK - WTR6955 debug
GPIO_19	CTS	GPIO_61	AUDIO_MI2S_MCLK	GPIO_103	RFFE2_DATA
GPIO_20	FP_SUB_RESET	GPIO_62	DBMD_DVDD_EN	GPIO_104	RFFE2_CLK
GPIO_21	SMB_STAT	GPIO_63	DBM_RSTN	GPIO_105	PRX_TUNER_SW1
GPIO_22	BLSP_I2C_SDA_6	GPIO_64	NC	GPIO_106	PRX_TUNER_SW2
GPIO_23	BLSP_I2C_SCL_6	GPIO_65	DBM_INT	GPIO_107	RFFE4_DATA
GPIO_24	IR_LED_EN	GPIO_66	TP_RESET_N	GPIO_108	RFFE4_CLK
GPIO_25	NC	GPIO_67	TP_INT_N	GPIO_109	RFFE5_DATA
GPIO_26	NC	GPIO_68	ACC_GYRO_INT1	GPIO_110	RFFE5_CLK
GPIO_27	NC	GPIO_69	ACC_GYRO_INT2	GPIO_111	PRX_TUNER_SW3
GPIO_28	BLSP_SPI8_MOSI	GPIO_70	HALL_EINT2	GPIO_112	NC
GPIO_29	BLSP_SPI8_MISO	GPIO_71	ALSP_INT_N	GPIO_113	NC
GPIO_30	BLSP_SPI8_CS_N	GPIO_72	FP_INT_N_1	SSC_0	NC
GPIO_31	BLSP_SPI8_CLK	GPIO_73	AUDIO_INT	SSC_1	LPI_PWR_EN
GPIO_32	CAM_MCLK0	GPIO_74	ANT_CHECK	SSC_2	LPI_I2C_3_SDA
GPIO_33	CAM_MCLK1	GPIO_75	HSJ_US_EURO_SEL	SSC_3	LPI_I2C_3_SCL
GPIO_34	NC	GPIO_76	HALL_EINT1	SSC_4	NC
GPIO_35	CAM_MCLK2	GPIO_77	AUDIO_PA_RST	SSC_5	NC
GPIO_36	CCI_I2C_SDA0	GPIO_78	WMSS_RESETN	SSC_6	NC
GPIO_37	CCI_I2C_SCL0	GPIO_79	SDM_HAPT_PWM	SSC_7	NC
GPIO_38	CCI_I2C_SDA1	GPIO_80	AUDIO_SEL	SSC_8	NC
GPIO_39	CCI_I2C_SCL1	GPIO_81	COEX_RXD	SSC_9	NC
GPIO_40	GPIO40_ID3	GPIO_82	COEX_TXD	SSC_10	NC
GPIO_41	FL_STROBE_TRIG	GPIO_83	UIM2_DATA	SSC_11	NC

SSC_12	SENS_RXD
SSC_13	SENS_TXD
SSC_14	NC
SSC_15	NC
SSC_16	NC
SSC_17	NC
SSC_18	WCD_SDM_MCLK
SSC_19	LPI_AUD_SB_CLK
SSC_20	LPI_AUD_SB_DATA0
SSC_21	LPI_AUD_SB_DATA1
SSC_22	LPI_AUD_CDC_INT1
SSC_23	LPI_AUD_CDC_INT2
SSC_24	LPI_AUD_CDC_RSTN
SSC_25	NC
SSC_26	NC
SSC_27	NC
SSC_29	NC
SSC_30	LPI_QCA_SB_CLK
SSC_31	LPI_QCA_SB_DATA0

GROOT GPIO Configuration For Starlord

GPIO_1	OPTION1	GPIO_8	SLB
GPIO_2	DIV_CLK2	GPIO_9	uUSB_TYPEC
GPIO_3	DIV_CLK1	GPIO_10	WCSS_VCTRL
GPIO_4	NFC_CLK_REQ	GPIO_11	HOMEKEY_FP_PM_INT
GPIO_5	WLAN_SW_CTRL	GPIO_12	WIPWR_MODE
GPIO_6	SLP_CLK	GPIO_13	PM_A_GPIO_13
GPIO_7	UIM_BATT_ALARM		

DRAX GPIO Configuration For Starlord

GPIO_1	OPTION2	GPIO_8	SD_CARD_DET_N
GPIO_2	LPI_PWR_EN	GPIO_9	WCSS_VCTRL
GPIO_3	FRONT_CAM_DVDD_EN	GPIO_10	SLB
GPIO_4	REAR_CAM_DVDD_EN	GPIO_11	LP4x_CTRL
GPIO_5	NC	GPIO_12	LP4x_MODE
GPIO_6	FP_VDD_EN		
GPIO_7	KEY_VOL_UP_N		

COMPANY: <Company Name>				
TITLE: <Title>				
DRAWN: <Drawn By>	DATED: <Drawn Date>			
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0	DRAWING NO. <Drawing Number>
QUALITY CONTROL: <QC By>	DATED: <QC Date>			REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>			

SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE:

U201-A

[17,33,51,52]

CONTROL

[5] LNBBCLK1	AT30	CXO	
[5] LNBRCLK1_EN	AU31	CXO_EN	
[5,20] SLEEP_CLK	AV30	SLEEP_CLK	
[5] PON_RESET_N	AT32	RESIN_N	
[10] RESOUT_N	B22	RESOUT_N	
VREG_L13A_1P8	AU37	MODE_0	
	AV38	MODE_1	
[5] SDM_PS_HOLD	AU29	PS_HOLD	
	K38	SRST_N	
	G41	TCK	
	F40	TDI	
	G39	TDO	
	E40	TMS	
	J39	TRST_N	
	E17	UFS_RESET	
	F22	UFS_REF_CLK	
	A21	UFS_REXT	
	E25	UFS_RX0_M	
	F23	UFS_RX0_P	
	F19	UFS_TX0_M	
	F20	UFS_TX0_P	
	BA19	DNC_1	
	AY20	DNC_2	
	BA15	DNC_3	
	V38	DNC_4	
	U39	DNC_5	

SDC1_RCLK	B20	SDC1_RCLK	[10]
SDC1_CLK	A23	SDC1_CLK	[10]
SDC1_CMD	A19	SDC1_CMD	[10]
SDC1_DATA_0	C25	SDC1_DATA_0	[10]
SDC1_DATA_1	C19	SDC1_DATA_1	[10]
SDC1_DATA_2	C23	SDC1_DATA_2	[10]
SDC1_DATA_3	D26	SDC1_DATA_3	[10]
SDC1_DATA_4	D20	SDC1_DATA_4	[10]
SDC1_DATA_5	D22	SDC1_DATA_5	[10]
SDC1_DATA_6	C17	SDC1_DATA_6	[10]
SDC1_DATA_7	D18	SDC1_DATA_7	[10]
SDC2_CLK	H38		
SDC2_CMD	J37		
SDC2_DATA_0	H36		
SDC2_DATA_1	G37		
SDC2_DATA_2	L35		
SDC2_DATA_3	K36		
USB1_HS_DM	BA39	USB_HS_DM	[13]
USB1_HS_DP	AY38	USB_HS_DP	[13]
USB2_HS_DM	AT38		
USB2_HS_DP	AR39		
USB0_SS_RX_M	AY35		
USB0_SS_RX_P	AW35		
USB0_SS_TX_M	AW37		
USB0_SS_TX_P	AV36		
USB1_SS_RX_M	AV40		
USB1_SS_RX_P	AW41		
USB1_SS_TX_M	AW39		
USB1_SS_TX_P	AV40		
USB1_SS_REXT	AY34		
DNC_6	AT40		
USB1_HS_REXT	BA35		
USB2_HS_REXT	AR41		
SPMI_CLK	AR37	SPMI_CLK	[5,8]
SPMI_DATA	AT28	SPMI_DATA	[5,8]

Reserved for SDM660 Compatable

U201-I

[17,33,51,52]

CONTROL

[10] EB0_CA0_CS_0	D8	EB0_CS_0	
[10] EB0_CA0_CS_1	D16	EB0_CS_1	
[10] EB0_CA0_CK_C	E13	EB0_CK_C	
[10] EB0_CA0_CK_T	F14	EB0_CK_T	
[10] EB0_CA0_CKE_0	C5	EB0_CKE_0	
[10] EB0_CA0_CKE_1	C11	EB0_CKE_1	
[10] EB0_DM0_0	A7	EB0_DM_0	
[10] EB0_DM0_1	A13	EB0_DM_1	
[16] EB0_DQS_C_0	E7	EB0_DQS_0_C	
[16] EB0_DQS_T_0	D6	EB0_DQS_0_T	
[10] EB0_DQS_C_1	D14	EB0_DQS_1_C	
[10] EB0_DQS_T_1	F15	EB0_DQS_1_T	
[10] EB0_CA0_CA_0	D12	EB0_CA_0	
[10] EB0_CA0_CA_1	E11	EB0_CA_1	
[10] EB0_CA0_CA_2	E5	EB0_CA_2	
[10] EB0_CA0_CA_3	F8	EB0_CA_3	
[10] EB0_CA0_CA_4	E9	EB0_CA_4	
[10] EB0_CA0_CA_5	D4	EB0_CA_5	

EB0_DQ_0	C1	EB0_DQ_0	[10]
EB0_DQ_1	B2	EB0_DQ_1	[10]
EB0_DQ_2	B4	EB0_DQ_2	[10]
EB0_DQ_3	A5	EB0_DQ_3	[10]
EB0_DQ_4	A3	EB0_DQ_4	[10]
EB0_DQ_5	A1	EB0_DQ_5	[10]
EB0_DQ_6	B8	EB0_DQ_6	[10]
EB0_DQ_7	A9	EB0_DQ_7	[10]
EB0_DQ_8	B16	EB0_DQ_8	[10]
EB0_DQ_9	B18	EB0_DQ_9	[10]
EB0_DQ_10	A17	EB0_DQ_10	[10]
EB0_DQ_11	A15	EB0_DQ_11	[10]
EB0_DQ_12	B14	EB0_DQ_12	[10]
EB0_DQ_13	A11	EB0_DQ_13	[10]
EB0_DQ_14	B12	EB0_DQ_14	[10]
EB0_DQ_15	B10	EB0_DQ_15	[10]

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[17,33,51,52]

CONTROL

[10] EB1_CA0_CS_0	D24	EB1_CS_0	
[10] EB1_CA0_CS_1	D32	EB1_CS_1	
[10] EB1_CA0_CK_C	F29	EB1_CK_C	
[10] EB1_CA0_CK_T	F28	EB1_CK_T	
[10] EB1_CA0_CKE_0	C37	EB1_CKE_0	
[10] EB1_CA0_CKE_1	C31	EB1_CKE_1	
[10] EB1_DM0_0	A35	EB1_DM_0	
[10] EB1_DM0_1	A29	EB1_DM_1	
[10] EB1_DQS_C_0	E35	EB1_DQS_0_C	
[10] EB1_DQS_T_0	D36	EB1_DQS_0_T	
[10] EB1_DQS_C_1	D28	EB1_DQS_1_C	
[10] EB1_DQS_T_1	E27	EB1_DQS_1_T	
[10] EB1_CA0_CA_0	D30	EB1_CA_0	
[10] EB1_CA0_CA_1	E31	EB1_CA_1	
[10] EB1_CA0_CA_2	E37	EB1_CA_2	
[10] EB1_CA0_CA_3	E34	EB1_CA_3	
[10] EB1_CA0_CA_4	E33	EB1_CA_4	
[10] EB1_CA0_CA_5	D34	EB1_CA_5	

EB1_CAL	D2	R209 240R 1%	DDR_VDDQ [10]
DDR_RESET_N	F39	DDR_RESET_N [10]	C204 1.0nF
EB1_DQ_0	C41	EB1_DQ_0	[10]
EB1_DQ_1	B41	EB1_DQ_1	[10]
EB1_DQ_2	B38	EB1_DQ_2	[10]
EB1_DQ_3	B36	EB1_DQ_3	[10]
EB1_DQ_4	A39	EB1_DQ_4	[10]
EB1_DQ_5	A37	EB1_DQ_5	[10]
EB1_DQ_6	B34	EB1_DQ_6	[10]
EB1_DQ_7	A33	EB1_DQ_7	[10]
EB1_DQ_8	B26	EB1_DQ_8	[10]
EB1_DQ_9	B24	EB1_DQ_9	[10]
EB1_DQ_10	A25	EB1_DQ_10	[10]
EB1_DQ_11	A27	EB1_DQ_11	[10]
EB1_DQ_12	B28	EB1_DQ_12	[10]
EB1_DQ_13	A31	EB1_DQ_13	[10]
EB1_DQ_14	B30	EB1_DQ_14	[10]
EB1_DQ_15	B32	EB1_DQ_15	[10]

U201-J

[17,33,51,52]

CONTROL

A1	GND_1	GND_51	U1
BA33	GND_2	GND_52	U41
M34	GND_3	GND_53	U7
F16	GND_4	GND_54	V32
F12	GND_5	GND_55	V34
F18	GND_6	GND_56	V38
F10	GND_7	GND_57	C13
V28	GND_8	GND_58	V20
V24	GND_9	GND_59	V22
M6	GND_10	GND_60	V24
M8	GND_11	GND_61	V26
U9	GND_12	GND_62	V28
BA37	GND_13	GND_63	V30
L5	GND_14	GND_64	V32
H8	GND_15	GND_65	V8
F36	GND_16	GND_66	W9
F38	GND_17	GND_67	Y34
F4	GND_18	GND_68	C15
F6	GND_19	GND_69	Y20
C21	GND_20	GND_70	Y22
C27	GND_21	GND_71	Y24
C29	GND_22	GND_72	Y26
C3	GND_23	GND_73	P14
BA41	GND_24	GND_74	P16
C33	GND_25	GND_75	R17
C35	GND_26	GND_76	R9
C39	GND_27	GND_77	AJ23
C7	GND_28	GND_78	AG27
C9	GND_29	GND_79	AF24
D18	GND_30	GND_80	AA13
D24	GND_31	GND_81	N25
D40	GND_32	GND_82	G35
E1	GND_33	GND_83	G5
E21	GND_34	GND_84	G7
BA7	GND_35	GND_85	H30
E3	GND_36	GND_86	J34
E41	GND_37	GND_87	J1
M34	GND_38	GND_88	J3
N15	GND_39	GND_89	J41
N41	GND_40	GND_90	AF26
P22	GND_41	GND_91	K30
P24	GND_42	GND_92	K4
P26	GND_43	GND_93	L15
P30	GND_44	GND_94	L19
P32	GND_45	GND_95	L3
R30	GND_46	GND_96	M10
T32	GND_47	GND_97	M12
T18	GND_48	GND_98	M14
T34	GND_49	GND_99	M16
T4	GND_50	GND_100	M2

U201-K

[17,33,51,52]

CONTROL

AF34	GND_101	GND_152	AR31
M20	GND_102	GND_153	AY14
M22	GND_103	GND_154	AA33
M24	GND_104	GND_155	AR35
M26	GND_105	GND_156	AR9
M30	GND_106	GND_157	AT16
M32	GND_107	GND_158	AT36
M38	GND_108	GND_159	AU3
AF29	GND_109	GND_160	AU35
AF30	GND_110	GND_161	AU39
A1	GND_111	GND_162	AU41
A41	GND_112	GND_163	AW8
AA1	GND_113	GND_164	AY16
AA35	GND_114	GND_165	AY1
AA41	GND_115	GND_166	AY11
AB24	GND_116	GND_167	AY19
AB26	GND_117	GND_168	BA13
AB28	GND_118	GND_169	BA17
AB34	GND_119	GND_170	BA21
AE35	GND_120	GND_171	BA25
AH8	GND_121	GND_172	AG33
AC31	GND_122	GND_173	AH14
AD10	GND_123	GND_174	AH16
AD12	GND_124	GND_175	BA1
AD14	GND_125	GND_176	AH18
AD26	GND_126	GND_177	AH20
AD34	GND_127	GND_178	AH24
AE18	GND_128	GND_179	AH28
AE24	GND_129	GND_180	AH34
AE28	GND_130	GND_181	AH8
AE41	GND_131	GND_182	AJ1
AE54	GND_132	GND_183	AJ19
AE7	GND_133	GND_184	AJ35
AF14	GND_134	GND_185	AJ41
AF16	GND_135	GND_186	BA29
AF18	GND_136	GND_187	AJ7
AN21	GND_137	GND_188	AK14
AN35	GND_138	GND_189	AK18
AN41	GND_139	GND_190	AK24
AN7	GND_140	GND_191	AK28
AP10	GND_141	GND_192	AK34
AW15	GND_142	GND_193	AK8
AP12	GND_143	GND_194	AL29
AP14	GND_144	GND_195	AL33
AP16	GND_145	GND_196	AL9
AP18	GND_146		
AP24	GND_147		
AP28	GND_148		
AP34	GND_149		
AP40	GND_150		
AR25	GND_151		

C205 100R_NO% 0201

R201 470R 1% 0201

R206 NC 0201

R208 0201

C203 22nF

R210 NC_10R 0201

R211 NC_10R 0201

R202 0201

DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number><Revision>	REV:
		SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND	SHEET 2 OF 2

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE:

U201-D
[17,33,51,52]
[17,33,51,52]
CONTROL

MIPI_CS0_CLK_P	[12]	AT2	MIPI_CS0_DC1K_P
MIPI_CS0_CLK_N	[12]	AR3	MIPI_CS0_DC1K_M
MIPI_CS0_DATA0_P	[12]	AR1	MIPI_CS0_DL N0_P
MIPI_CS0_DATA0_N	[12]	AP2	MIPI_CS0_DL N0_M
MIPI_CS0_DATA1_P	[12]	AN1	MIPI_CS0_DL N1_P
MIPI_CS0_DATA1_N	[12]	AM1	MIPI_CS0_DL N1_M
MIPI_CS0_DATA2_P	[12]	AM2	MIPI_CS0_DL N2_P
MIPI_CS0_DATA2_N	[12]	AL3	MIPI_CS0_DL N2_M
MIPI_CS0_DATA3_P	[12]	AL1	MIPI_CS0_DL N3_P
MIPI_CS0_DATA3_N	[12]	AK2	MIPI_CS0_DL N3_M
MIPI_CS1_CLK_P	[12]	AT4	MIPI_CS1_DC1K_P
MIPI_CS1_CLK_N	[12]	AU3	MIPI_CS1_DC1K_M
MIPI_CS1_DATA0_P	[12]	AU5	MIPI_CS1_DL N0_P
MIPI_CS1_DATA0_N	[12]	AV4	MIPI_CS1_DL N0_M
MIPI_CS1_DATA1_P	[12]	AV2	MIPI_CS1_DL N1_P
MIPI_CS1_DATA1_N	[12]	AW1	MIPI_CS1_DL N1_M
MIPI_CS1_DATA2_P	[12]	AW3	MIPI_CS1_DL N2_P
MIPI_CS1_DATA2_N	[12]	AY2	MIPI_CS1_DL N2_M
MIPI_CS1_DATA3_P	[12]	AY4	MIPI_CS1_DL N3_P
MIPI_CS1_DATA3_N	[12]	BA3	MIPI_CS1_DL N3_M
MIPI_CSI2_CLK_P	[12]	AR5	MIPI_CS2_DC1K_P
MIPI_CSI2_CLK_N	[12]	AP6	MIPI_CS2_DC1K_M
MIPI_CSI2_DATA0_P	[12]	AP4	MIPI_CS2_DL N0_P
MIPI_CSI2_DATA0_N	[12]	AN5	MIPI_CS2_DL N0_M
MIPI_CSI2_DATA1_P	[12]	AM6	MIPI_CS2_DL N1_P
MIPI_CSI2_DATA1_N	[12]	AL7	MIPI_CS2_DL N1_M
MIPI_CSI2_DATA2_P	[12]	AL5	MIPI_CS2_DL N2_P
MIPI_CSI2_DATA2_N	[12]	AK6	MIPI_CS2_DL N2_M
MIPI_CSI2_DATA3_P	[12]	AK4	MIPI_CS2_DL N3_P
MIPI_CSI2_DATA3_N	[12]	AJ5	MIPI_CS2_DL N3_M

MIPI_DSI0_CLK_N	AV37	MIPI_DSI0_CLK_N	[12]
MIPI_DSI0_CLK_P	AV38	MIPI_DSI0_CLK_P	[12]
MIPI_DSI0_LN0_N	AW36	MIPI_DSI0_LANE0_N	[12]
MIPI_DSI0_LN0_P	AG37	MIPI_DSI0_LANE0_P	[12]
MIPI_DSI0_LN1_N	AF38	MIPI_DSI0_LANE1_N	[12]
MIPI_DSI0_LN1_P	AF39	MIPI_DSI0_LANE1_P	[12]
MIPI_DSI0_LN2_N	AE37	MIPI_DSI0_LANE2_N	[12]
MIPI_DSI0_LN2_P	AY39	MIPI_DSI0_LANE2_P	[12]
MIPI_DSI0_LN3_N	AD36	MIPI_DSI0_LANE3_N	[12]
MIPI_DSI0_LN3_P	AC37	MIPI_DSI0_LANE3_P	[12]
MIPI_DSI0_REXT	AK40	1.40/1% 0.125W 1/8 R318	
MIPI_DSI1_CLK_N	AH40		
MIPI_DSI1_CLK_P	AG41		
MIPI_DSI1_LN0_N	AG39		
MIPI_DSI1_LN0_P	AF40		
MIPI_DSI1_LN1_N	AD40		
MIPI_DSI1_LN1_P	AC41		
MIPI_DSI1_LN2_N	AC39		
MIPI_DSI1_LN2_P	AB40		
MIPI_DSI1_LN3_N	AB38		
MIPI_DSI1_LN3_P	AA39		
MIPI_DSI1_REXT	AE41		
EDP_AUX_N	AE33		
EDP_AUX_P	AY34		

U201-H
[17,33,51,52]
[17,33,51,52]
CONTROL

[20] COEX_CLK		V6	WCSS_CXM_RFA_CMD_CLK
[20] COEX_DATA		U5	WCSS_CXM_RFA_CMD_DATA
[20] WL_CMD_CLK_C00		V4	WCSS1_BBD_RFA_CMD_CLK
[20] WL_CMD_DATA_C00		V6	WCSS1_BBD_RFA_CMD_DATA
		W7	WCSS2_BBD_RFA_CMD_CLK
		W5	WCSS2_BBD_RFA_CMD_DATA
[5,8] WCSS_VCTRL		M4	WLAN_PWR_EN
		L1	WLAN1_DAC_REXT
[20] WL_BB_IN_TX		J7	WLAN1_ADC_IM
[20] WL_BB_IP_TX		H6	WLAN1_ADC_IP
[20] WL_BB_QN_TX		K6	WLAN1_ADC_QM
[20] WL_BB_QP_TX		J5	WLAN1_ADC_QP
		K2	WLAN2_DAC_REXT
[20] WL_BB_IN_RX		F2	WLAN2_ADC_IM
[20] WL_BB_IP_RX		G1	WLAN2_ADC_IP
[20] WL_BB_QN_RX		H1	WLAN2_ADC_QM
[20] WL_BB_QP_RX		G3	WLAN2_ADC_QP

RF_SD_CLK	T2	WLAN_5G_CLK_OUT	[20]
QREFS_CXO_REXT	AY32	30.9/1% 0.125W 1/8 R319	
QUNK_CLK_M	AW17	QUNK_CLK_M	[15]
QUNK_CLK_P	AY16	QUNK_CLK_P	[15]
QUNK_DL0_M	AU15	QUNK_RX0_M	[15]
QUNK_DL0_P	AY14	QUNK_RX0_P	[15]
QUNK_DL1_M	AY14	QUNK_RX1_M	[15]
QUNK_DL1_P	AU13	QUNK_RX1_P	[15]
QUNK_DL2_M	AY12	QUNK_RX2_M	[15]
QUNK_DL2_P	AW13	QUNK_RX2_P	[15]
QUNK_CLK_M	AU17	QUNK_TX_M	[15]
QUNK_CLK_P	AV18	QUNK_TX_P	[15]

Reserved for SDM660 Compatiable
0.04K/1% 0.125W 1/8 R320

U201-C
[17,33,51,52]
[17,33,51,52]
CONTROL

[8] LPI_PWR_EN		AJ1	LPI_GPIO_0
[3,14] I2C_SENSORS_SDA		AH4	LPI_GPIO_1
[3,14] I2C_SENSORS_SCL		AC1	LPI_GPIO_2
		AD2	LPI_GPIO_3
		AH6	LPI_GPIO_4
		AC5	LPI_GPIO_5
		AC3	LPI_GPIO_6
		AF6	LPI_GPIO_7
		AG4	LPI_GPIO_8
		AF2	LPI_GPIO_9
		AH2	LPI_GPIO_10
		AG1	LPI_GPIO_11
[20] SENS_RXD		U3	LPI_GPIO_12
[20] SENS_TXD		V4	LPI_GPIO_13
		W3	LPI_GPIO_14
		Y2	LPI_GPIO_15
		AF3	LPI_GPIO_16
		AF4	LPI_GPIO_17
[9] LPI_CDC_PDM_CLK		AA1	LPI_GPIO_18
[9] LPI_CDC_PDM_SYNC		AA5	LPI_GPIO_19
[9] LPI_CDC_PDM_TX		AB6	LPI_GPIO_20
[9] LPI_CDC_PDM_RX0		AC7	LPI_GPIO_21
[9] LPI_CDC_PDM_RX0_DRE		AC9	LPI_GPIO_22
[9] LPI_CDC_PDM_RX1		AD6	LPI_GPIO_23
[9] LPI_CDC_PDM_RX1_DRE		AD4	LPI_GPIO_24
[9] LPI_CDC_PDM_RX2		AE5	LPI_GPIO_25
		AA3	LPI_GPIO_26
		AB4	LPI_GPIO_27
		AB2	LPI_GPIO_28
		AC4	LPI_GPIO_29
[20] SB_CLK		W1	LPI_GPIO_30
[20] SB_DATA		Y1	LPI_GPIO_31

U201-B
[17,33,51,52]
[17,33,51,52]
CONTROL

[11] DBM_UART0_RXD	TXD	AK36	GPIO_0
DBM_UART0_TXD	RXD	AL35	GPIO_1
[3,12] I2C_TP_SDA		AL37	GPIO_2
[3,12] I2C_TP_SCL		AM36	GPIO_3
	TP11	AN39	GPIO_4
	TP10	AP38	GPIO_5
[3,7,10] BLSP2_I2C_SDA		AJ39	GPIO_6
[3,7,10] BLSP2_I2C_SCL		AK38	GPIO_7
[14] BLSP_SPI3_MOSI		V36	GPIO_8
[14] BLSP_SPI3_MISO		W35	GPIO_9
[14] BLSP_SPI3_CS_N		W37	GPIO_10
[14] BLSP_SPI3_CLK		V36	GPIO_11
[11] AUDIO_MI2S_SCK		K40	GPIO_12
[11] AUDIO_MI2S_WS		L39	GPIO_13
[11] AUDIO_MI2S_D0		L41	GPIO_14
[11] AUDIO_MI2S_D1		M40	GPIO_15
[20] RXD		P6	GPIO_16
[20] TXD		R7	GPIO_17
[20] RTS		P8	GPIO_18
[20] CTS		N7	GPIO_19
[14] FP_SUB_RESET		U35	GPIO_20
[7] SMB_STAT		AM38	GPIO_21
[3,11] BLSP_I2C_SDA_6		P4	GPIO_22
[3,11] BLSP_I2C_SCL_6		N3	GPIO_23
[14] IR_LED_EN		M36	GPIO_24
		N37	GPIO_25
		L37	GPIO_26
		M39	GPIO_27

For Voice wake up IC

[11] BLSP_SPI8_MOSI	MOSI	R3	GPIO_28
[11] BLSP_SPI8_MISO	MISO	N5	GPIO_29
[11] BLSP_SPI8_CS_N	CS_N	P2	GPIO_30
[11] BLSP_SPI8_CLK	CLK	R1	GPIO_31
[12] CAM_MCLK0	R327 22/[1] 0R	AU9	GPIO_32
[12] CAM_MCLK1	R328 22/[1] 0R	AV6	GPIO_33
		AU8	GPIO_34
[12] CAM_MCLK2	R329 22/[1] 0R	AW5	GPIO_35
[3,12] CCI_I2C_SDA0		BA1	GPIO_36
[3,12] CCI_I2C_SCL0		AY8	GPIO_37
[3,12] CCI_I2C_SDA1		AU2	GPIO_38
[3,12] CCI_I2C_SCL1		AT8	GPIO_39
[3] GPO40_IO3		AT10	GPIO_40
[8] FL_STROBE_TRIG		AR11	GPIO_41
[3] ID0		AV10	GPIO_42
[3] ID1		BA11	GPIO_43
[3] ID2		AY6	GPIO_44
DBM_AF_VDD_20K_EN		AU11	GPIO_45
[12] REAR_CAM_DVDD_EN_2		AW7	GPIO_46
[12] CAM1_RST_N		AT6	GPIO_47
[12] CAM2_RST_N		AY12	GPIO_48
[12] LDM_IDO		AR7	GPIO_49
[12] CAM_AF_VDD_EN		AW11	GPIO_50
[12] CAM_AVDD_EN		AW9	GPIO_51
[12] CAM3_RST_N		AY10	GPIO_52
[12] LCD_RESET		Y36	GPIO_53
SD_CARD_DET_N		U33	GPIO_54
[12] LDM_ID1		AW33	GPIO_55
[13] ACOK		AW35	GPIO_56

GPIO_57	AN37	FORCED_USB_BOOT	[13]
GPIO_58	AV32	USB_PHY_PS	[6]
GPIO_59	M41	LCD_TE	[12]
GPIO_60	AA37		
GPIO_61	N35	AUDIO_MI2S_MCLK	
GPIO_62	Y40	DBMD_DVDD_EN	[11]
GPIO_63	N39	DBM_RSTN	[11]
GPIO_64	AL39		
GPIO_65	AT12	DBM_INT	[11]
GPIO_66	Y40	TP_RESET_N	[12]
GPIO_67	W39	TP_INT_N	[12]
GPIO_68	P38	ACC_GYRO_INT1	[14]
GPIO_69	P40	ACC_GYRO_INT2	[14]
GPIO_70	R39		
GPIO_71	R41	ALSP_INT_N	[14]
GPIO_72	T40	FP_INT_N_3	[14]
GPIO_73	P36	AUDIO_INT	[11]
GPIO_74	R35	ANT_CHECK	[18]
GPIO_75	R37	HSJ_US_EURO_SEL	[13]
GPIO_76	T36	HALL_EINT1	[13]
GPIO_77	T38	AUDIO_PA_RST	[11]
GPIO_78	U37	WMSS_RESETN	[15]
GPIO_79	AY18	SDM_HAPT_PWM	[6]
GPIO_80	AW19	AUDIO_SEL	[11,13]
GPIO_81	R5	COEX_RXD	[20]
GPIO_82	T6	COEX_TXD	[20]
GPIO_83	AY26	U9M2_DATA	[13]
GPIO_84	BA27	U9M2_CLK	[13]
GPIO_85	AW27	U9M2_RESET	[13]
GPIO_86	AY28	U9M2_PRESENT	[13]
GPIO_87	AY28	U9M1_DATA	[13]
GPIO_88	AW29	U9M1_CLK	[13]
GPIO_89	AY30	U9M1_RESET	[13]
GPIO_90	BA31	U9M1_PRESENT	[13]
GPIO_91	AW25	UIM_BATT_ALARM	[5]
GPIO_92	AY20	DRX_TUNER_SW0	[13]
GPIO_93	AW21	DRX_TUNER_SW1	[13]
GPIO_94	AY22	DRX_TUNER_SW2	[13]
GPIO_95	BA23	PRX_TUNER_SW5	[13]
GPIO_96	AW23	PRX_TUNER_SW6	[13]
GPIO_97	AY24	DRX_TUNER_SW5	
GPIO_98	AY24	PRX_TUNER_SW4	[13]
GPIO_99	AT18	QUNK_REQUEST	[15]
GPIO_100	AU19	QUNK_ENABLE	[15]
GPIO_101	AR19	RFFE1_DATA	[15]
GPIO_102	AT35	RFFE1_CLK	[15]
GPIO_103	AG21	RFFE2_DATA	[19]
GPIO_104	AY22	RFFE2_CLK	[19]
GPIO_105	AT22	PRX_TUNER_SW1	[13]
GPIO_106	AU23	PRX_TUNER_SW2	[13]
GPIO_107	AR23	RFFE4_DATA	[19]
GPIO_108	AT24	RFFE4_CLK	[19]
GPIO_109	AU25	RFFE5_DATA[16,18]	
GPIO_110	AY26	RFFE5_CLK [16,18]	
GPIO_111	AT26	PRX_TUNER_SW3	[13]
GPIO_112	AU27	LNA_PRX_B41_EN	[18,19]
GPIO_113	AM40		

GPIO58 GND for uUSB.
GPIO58 PM660 39 pin for Type C

RF_ANT_CHECK

HSJ_US_EURO_SEL

Reserved for main antenna tuner
Reserved for diversity antenna tuner

sensor I2C

camera I2C

SMB I2C

Smart I2C

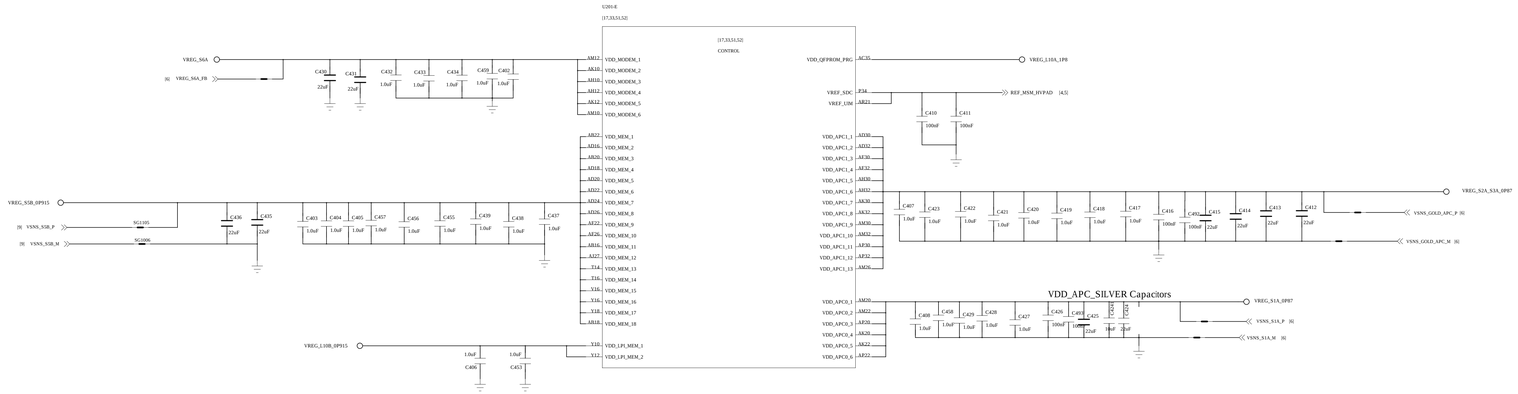
LEGACY TOUCH

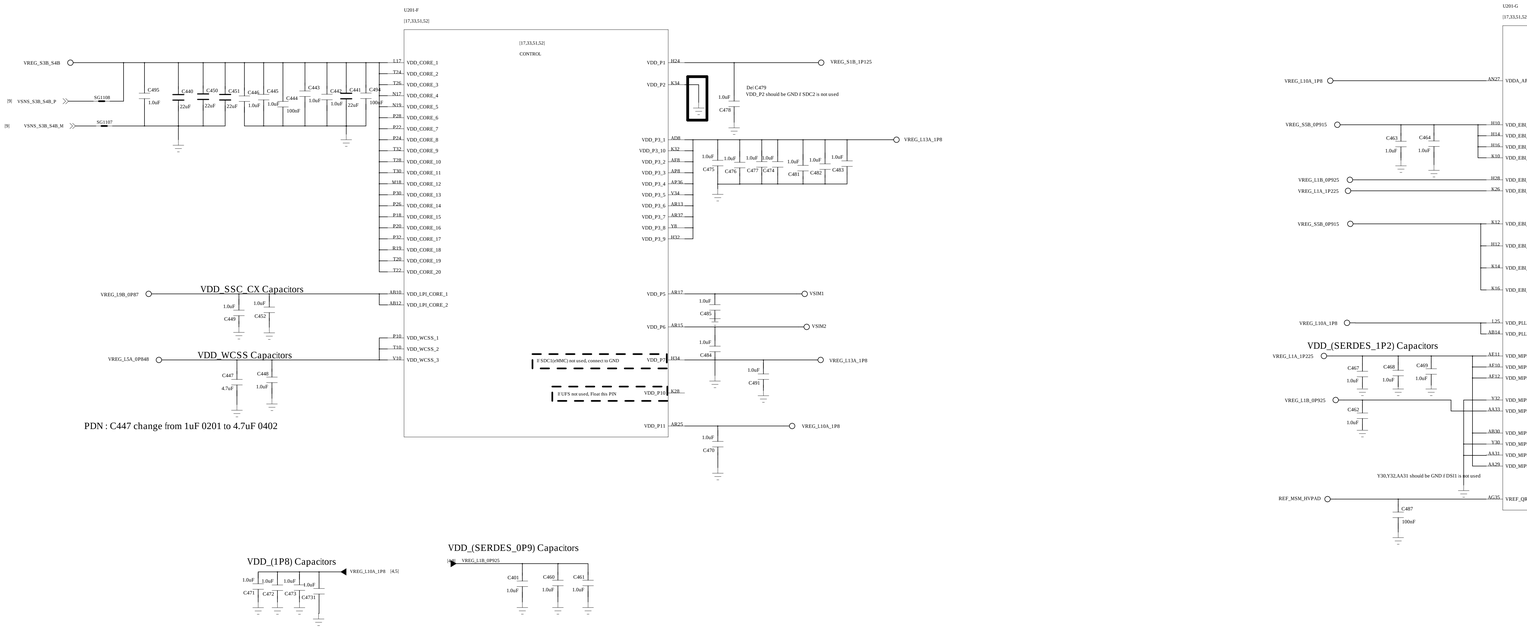
Board ID

[3] ID0	R322	R321	R311
[3] ID1	100K	100K	100K
[3] ID2	R318	R317	R316
GPO40_ID3	100K	100K	100K

COMPANY:	<Company Name>			
TITLE:	<Title>			
DRAWN: <Drawn By>	DATED: <Drawn Date>			
CHECKED: <Checked By>	DATED: <Checked Date>			
QUALITY CONTROL: <QC By>	DATED: <QC Date>			
RELEASED: <Released By>	DATED: <Release Date>	CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number><Revision>
		SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND	REV:

REVISION RECORD			
LTR	ECO NO.	APPROVED	DATE.





PDN : C447 change from 1uF 0201 to 4.7uF 0402

PDN：C465 C489 change to 2.2uF---0928

COMPANY: <Company Name>			
TITLE: <Title>			
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND		

REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
Dedicated to main GND plane
CAD NOTE: VIA DIRECTLY TO MAIN GND. DON'T CONNECT TO ANY OTHER GND
P-type are pseudo-capless, cap can be at load.
Regulators used internal to PMIC need cap at PMIC.
N-type = N300 need cap at PMIC
FOR SDM660 , GPIO_1 is HI-Z
FOR SDM630 , GPIO_1 is low
PMK_Sleep_CLK
uUSB_TYPEC is Hi-Z for TypeC
uUSB_TYPEC is LOW for uUSB
PLACE CLOSE TO SDM
COMPANY:
<Company Name>
TITLE:
<Title>
DRAWN:
<Drawn By>
DATED:
<Drawn Date>
CHECKED:
<Checked By>
<Checked Date>
QUALITY CONTROL:
<QC By>
<QC Date>
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A0
<Drawing Number>
<Revision>
SCALE:

REVISION RECORD			
LTR	ECO NO	APPROVED	DATE

U501-F

VPH_PWR BULK CAPS. DISTRIBUTE THESE ALL OVER U501

VPH_PWR
C619 22uF
C611 22uF
C612 22uF
C613 22uF
C614 22uF

VDD_S1_1 65
VDD_S1_2 66
GND_S1_3 86
GND_S1_2 87
C616 2.2uF
Dedicated to main GND plane

VDD_S2_1 33
VDD_S2_2 55
GND_S2_1 10
GND_S2_2 32
C602 2.2uF
Dedicated to main GND plane

VDD_S3_1 20
VDD_S3_3 42
VDD_S3_2 21
VDD_S3_4 43
C603 2.2uF
Dedicated to main GND plane

VDD_S4_1 175
VDD_S4_2 186
VDD_S4_3 208
GND_S4_1 196
GND_S4_2 207
C604 2.2uF
Dedicated to main GND plane

VDD_S5_1 131
VDD_S5_2 141
GND_S5_1 163
GND_S5_2 164
C607 2.2uF
Dedicated to main GND plane

VDD_S6 120
GND_S6 97
C615 2.2uF
Dedicated to main GND plane

[1,16,17,45] HK

VREG_S1 96 — VSNS_S1A_P [4]
VSW_S1_1 75
VSW_S1_2 76
VSW_S1_3 77
L603 0.47uH — VREG_S1A_SW [4]
VREF_NEG_S1 107 — VSNS_S1A_M [4]

VREG_S2 95
VSW_S2_1 11
VSW_S2_2 22
VSW_S2_3 44
VSW_S2_4 54
L602 0.47uH — VREG_S2A_S3A_DPRT
VREF_NEG_S2 85 — VSNS_GOLD_APC_M [4]
VREG_S3 74 — VSNS_GOLD_APC_P [4]
VSW_S3_1 9
VSW_S3_2 31
VSW_S3_3 53
L603 0.47uH
VREF_NEG_S3 73

VREG_S4 174
VSW_S4_1 185
VSW_S4_2 197
VSW_S4_3 219
L604 1uH — VREG_S4A
22uF C605
22uF C606
Dedicated to main GND plane

VREG_S5 162
VSW_S5_1 142
VSW_S5_2 153
L605 1uH — VREG_S5A [5]
22uF C608
22uF C609
Dedicated to main GND plane

VREG_S6 119 — VREG_S6A_FB [4]
VSW_S6_1 98
VSW_S6_2 109
L606 1uH — VREG_S6A [4]

CHG_GND connect together , then Dedicated to main GND plane

U501-S

[6,7,13] USB_VBUS — C617 4.7uF_25V — USB_IN_1 78, USB_IN_2 79, USB_IN_3 80, USB_IN_4 89
USB_IN_MID_1 56, USB_IN_MID_2 57, USB_IN_MID_3 67, USB_IN_MID_4 68 — 4.7uF_25V C618 — GND

VPH_PWR — VCONN_IN 17, VCONN_EN 61
[11,13] USB_CC1 — CC1_ID 5
[13] USB_CC2 — CC2 27
[3] USB_PHY_PS — CC_OUT 59
[7] STAT_CHG — STAT_CHG 90
C625 220pF, C626 220pF

WIPWR_RECHG 92
WIPWR_CHG_OK 91
QI_PMA_ON 103

LDO_CTRL_1 1
LDO_CTRL_2 2
DC_EN 99
DC_SNS 86
USB_EN 100
[6,7,9] USB_VBUS — USB_SNS 101
[13] USB_HS_DP_PM — USB_DP 45
[13] USB_HS_DM_PM — USB_DM 60
[13] VBATT_CONN_VSNS_M — VBATT_SNS_M 81
[13] VBATT_CONN_VSNS_P — VBATT_SNS_P 102
[13] VBATT_CONN_ISNS_M — IBATT_SNS_M 133
[13] VBATT_CONN_ISNS_P — IBATT_SNS_P 122
0R R603 (NS) — ISNS_SMB_M 155
0R R604 (NS) — ISNS_SMB_P 144
[13] BATT_ID — BATT_ID 113
[13] BATT_THERM — BATT_THERM 166
VREG_LSA_1P8 — AUX_THERM 177
[8] BA_N — BA_N 157
GND_FG 134
REF_GND_FG 167
GND_PSUB_FG 124
[11,16,17,45] HK

Note:R1804 should the value of RT1801 at 45@ degree
[8] AUX_THERM_BIAS — R1804 470KFT 1% 1/16W
R1805 470K 1% NTC
RT1 is for device skin temp monitor,Using charging
Dedicated to main GND plane

Dedicated to main GND plane

BOOT_QTI 36
C623 27nF 16V
VSW_CHG_1 37
VSW_CHG_2 38
VSW_CHG_3 45
VSW_CHG_4 46
L607 1uH
C624 22uF, C619 33pF — VPH_PWR
PGND_CHG_1 12
PGND_CHG_2 13
PGND_CHG_3 23
PGND_CHG_4 24
Dedicated to main GND plane

VPH_PWR1 3
VPH_PWR2 15
VPH_PWR3 25
VPH_PWR4 37
VPH_PWR5 47

VBATT_PWR_1 4 — VBATT [13]
VBATT_PWR_2 16
VBATT_PWR_3 26
VBATT_PWR_4 38
VBATT_PWR_5 48
10uF C620

BATT_THERM_BIAS 156 — BATT_THERM_BIAS [13]
AUX_THERM_BIAS 145 — AUX_THERM_BIAS [8]

VAIB 112
C621 100nF
C622 1.5uF
VREG_FG 123
BOOT_PWR 14 — BOOT_PWR [7]
REF_GND_CHG 59
4.7uF
Dedicated to main GND plane
Dedicated to main GND plane

GND connect together , then Dedicated to main GND plane

COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN: <Drawn By>	DATED: <Drawn Date>	CODE: <Code>	SIZE: A0
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		

SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND

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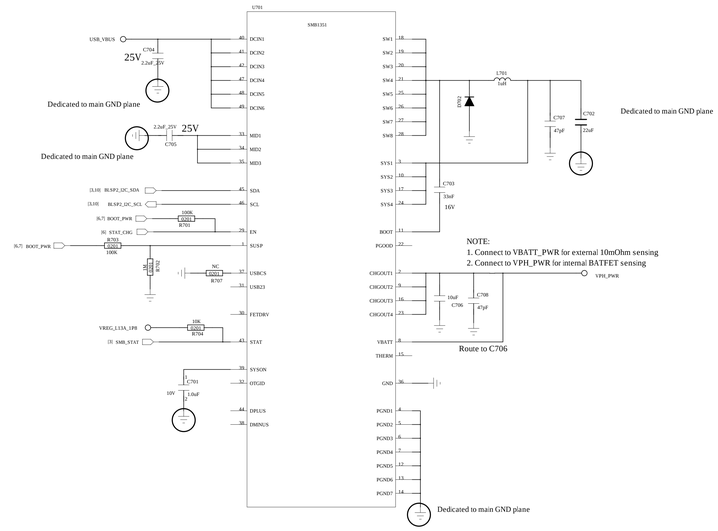
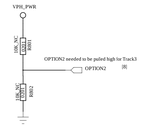
LTR	ECO NO	APPROVED	DATE

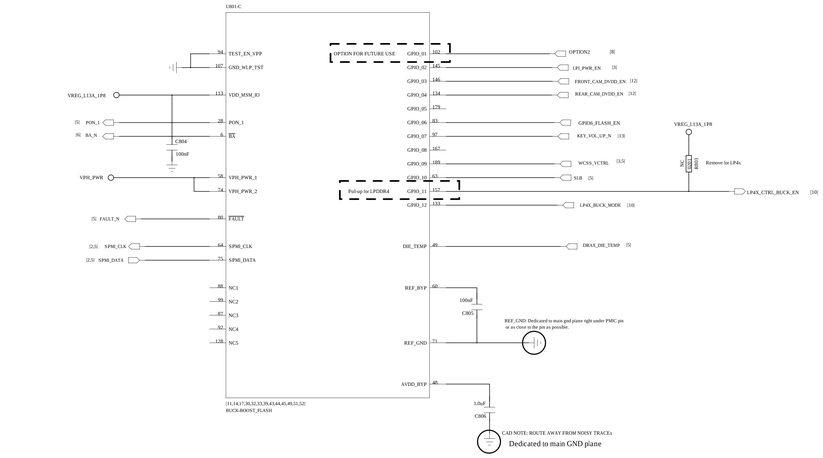


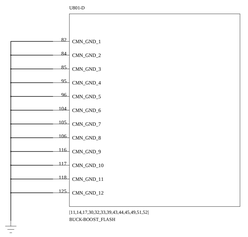
DRAWN: <Drawn By>	DATED: <Drawn Date>
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

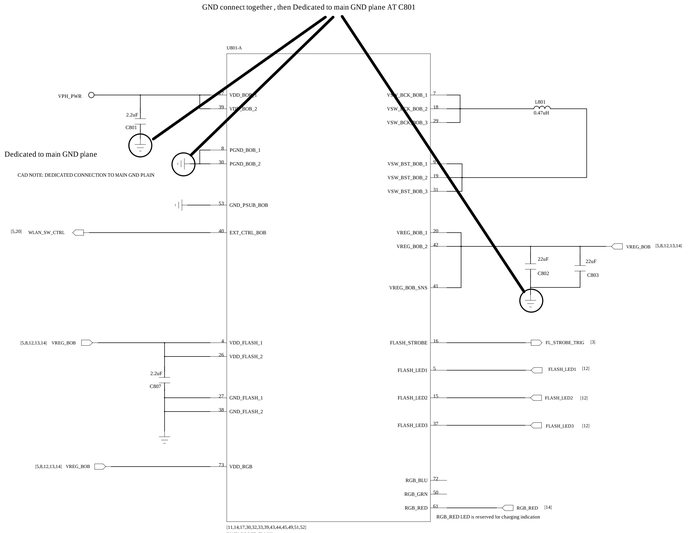
COMPANY: <Company Name>			
TITLE: <Title>			
CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND, DO NOT CONNECT TO ANY OTHER GND		

REVISION RECORD			
LTR	ECO NO	APPROVED	DATE

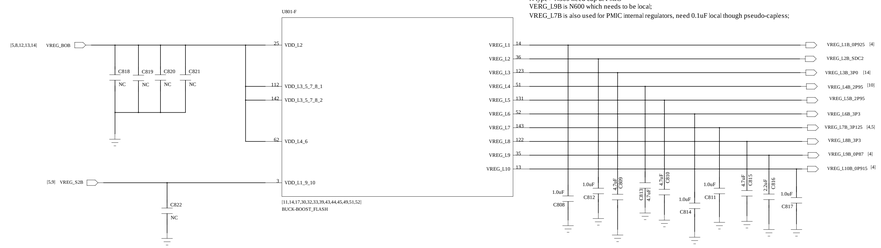








P-type are psuedo-capless, cap can be at load.
Regulators used internal to PMIC need cap at PMIC.
N-type > N300 need cap at PMIC
VERG_L9B is N600 which needs to be local;
VREG_L7B is also used for PMIC internal regulators, need 0.1uF local though pseudo-capless;

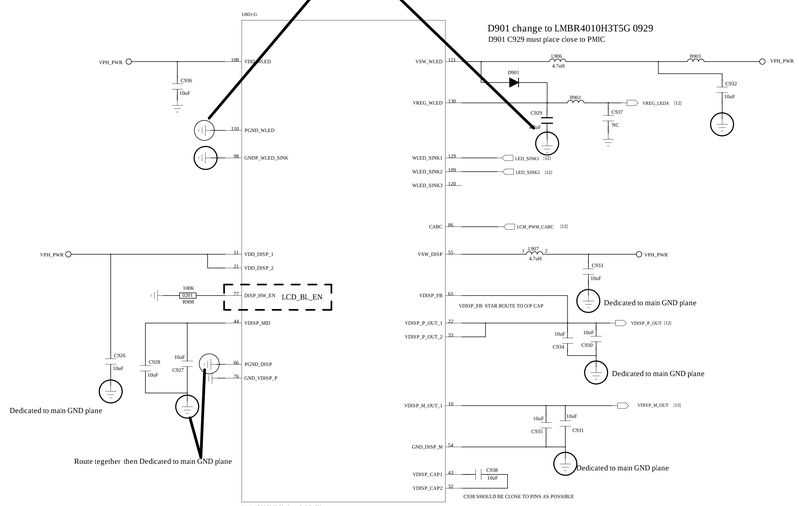


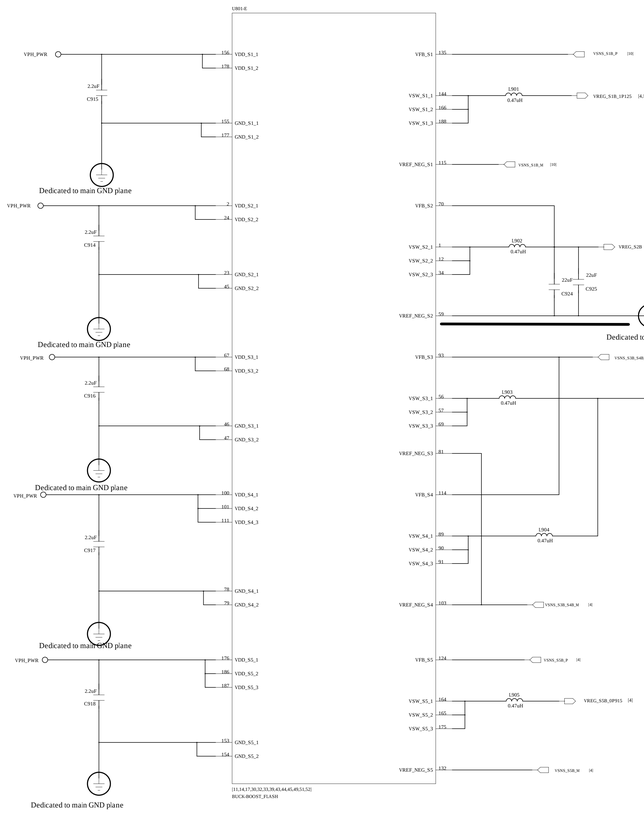
REVISION RECORD			
LTR	ECO NO	APPROVED	DATE

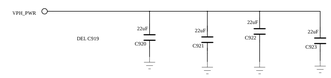
GND connect together , then Dedicated to main GND plane AT C929

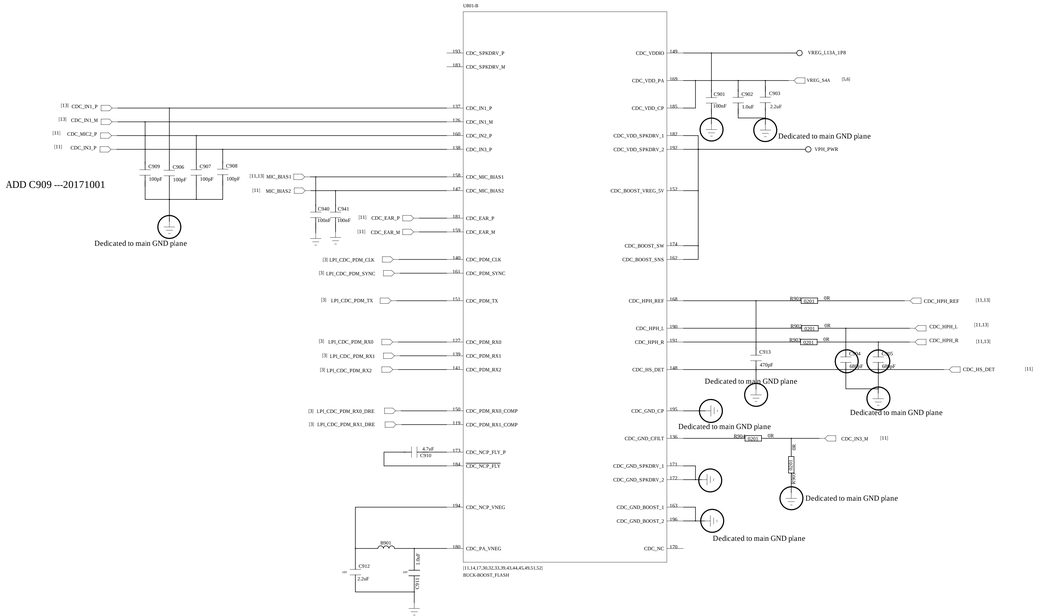
D901 change to LMBR4010H3T5G 0929

D901 C929 must place close to PMIC









COMPANY: <Company Name>					
TITLE: <Title>					
DRAWN: <Drawn By>	DATED: <Drawn Date>				
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>	SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND		

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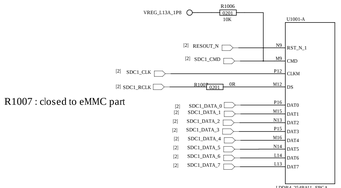
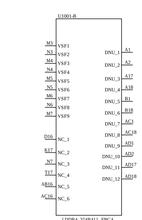
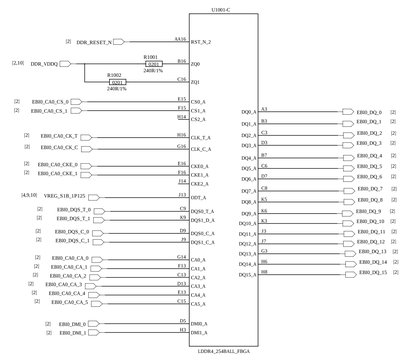
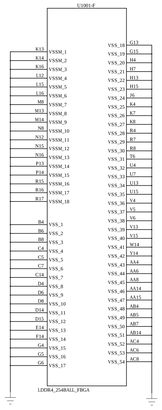
LTR	ECO NO	APPROVED	DATE

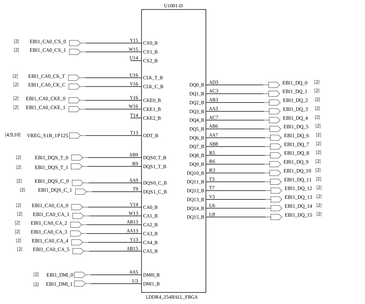


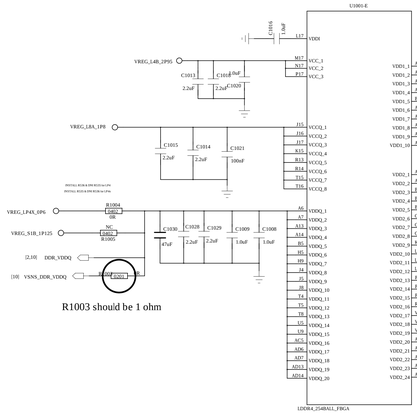
R1007 : closed to eMMC part







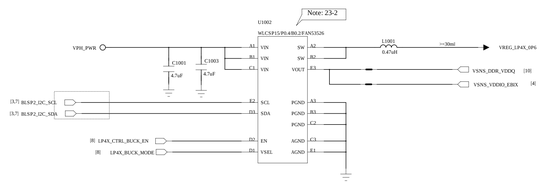




R1003 should be 1 ohm

Buck for VDRAM

FAN53526 / Buck I2C address: 0X60 (Write:0xC0, Read:0xC1)

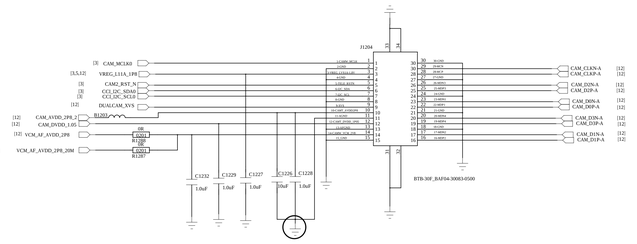


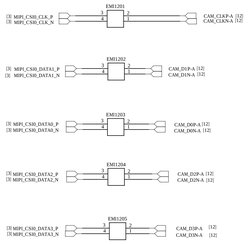
DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
		SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND


Sub MIC
MIC_BIAS1
MIC101
OUT
POWER
GND
GND
GND
AM0502B-NE381-X01
B1101 180nH
B1102 180nH
B1103 180nH
B1106 180nH
C1101 100nF
C1102 100pF
C1103 33pF
C1104 33pF
C1109 NC
T1102
T1107
C1126 1.0uF
C1127 1.0uF
DBM_IN3_P [11]
DBM_INT3_M [11]
CDC_IN3_P [9]
CDC_IN3_M [9]
together then single via to main GND
Smart PA
NC TP26 NC TP27 NC TP28 NC TP29
[3,11] AUDIO_MI2S_SCK
[3,11] AUDIO_MI2S_WS
[3,11] AUDIO_MI2S_D0
[3,11] AUDIO_MI2S_D1
[3] BLSP_I2C_SCL_6
[3] BLSP_I2C_SDA_6
[3,11] AUDIO_INT
[3,11] AUDIO_PA_RST
U1160
TAS2555
IN_P
IN_M
MCLK_GPI2
BCLK1_GPIO1
WCLK1_GPIO2
DIN1_GPI1
DOUT1_GPIO3
BCLK2_GPIO5
WCLK2_GPIO6
DIN2_GPIO8
DOUT2_GPIO7
SCL_SSZ
SDA_MOSI
IRQ_GPIO4
/RESET
ICC_GPI3
ICC_GPIO9
ICC_GPIO10
ADR1_MISO
ADR0_SCLK
SPI_SELECT
SW
SW
VBAT
DVDD
AVDD
IOVDD
VREG
VBOOST
VBOOST
SPK_P
SPK_M
VSENSE_P
VSENSE_M
NC
NC
PGND
PGND_B
PGND_B
IOGND
AGND
DGND
VPH_PWR
VREG_L13A_1P8
L1160 1uH
C1160 10nF
C1161 10uF
C1162 100nF
C1163 100nF
C1164 100nF
C1165 100nF
C1166 10uF 16V
C1167 10uF
C1168 100pF
C1169
C1170
Connect to PGND_B together
R1162 0603 0R
R1164 0201 NC
R1163 0603 0R
R1165 0201 NC
SPKR_OUT_P [13]
SPKR_OUT_M [13]
VSENSE_P [13]
VSENSE_M [13]
R1160 0201 10K
R1161 0201 10K
REC
REC1101
B1104
B1105
C1111 100pF
C1112 33pF
C1113 33pF
T1103
T1104
CDC_EAR_M [9]
CDC_EAR_P [9]
[11] DBMD_DVDD_1.1
THIS VOL SHOULD ON
VREG_L13A_1P8 [2,3,4,5,6,7,8,9,10,11,13,14,15,16,18,19,20]
R1125 0201 0R
R1124 0201 0R
R1121 0201 0R
C1130 1.0uF
C1131 100nF
C1132 1.0uF
1.8V
1.8V
1.1V
VCCA
VDD_IO
VDD_CORE
R1130 0201 10K
[5] DBM_CLK slpp_clk??
[3] DBM_INT
[3] DBM_RSTN
NC TP33 NC TP34 NC TP31 NC TP32
NC TP14
NC TP30
C1108 1.0uF
[3] DBM_UART0_RXD
R1122 0201 0R
[3] BLSP_SPI8_CLK
[3] BLSP_SPI8_CS_N
[3] BLSP_SPI8_MOSI
[3] BLSP_SPI8_MISO
R1126 0201 0R
R1127 0201 0R
R1128 0201 0R
R1129 0201 0R
MASTER_CLK
GPIO14/TDM0_FSYNC/DM1_CLK/UART1_TXD
RSTN
GPIO12/DM1_CLK/UART0_RTS/TDO
GPIO11/DM1_DATA/TCK
GPIO17/UART0_TXD/DM1_CLK
GPIO18/UART0_RXD/WAKEUP/DM1_DATA
GPIO6/SPI_CLK/IIC_SCL1/DM0_CLK
GPIO7/SPI_SCS/IIC_SDA1
GPIO5/SPI_SDI/DM0_DATA
GPIO4/SPI_SDO/CLKOUT_P
GPIO1/IIC_SCL0/DM1_DATA/GPIO22/CLKOUT_N
GPIO2/IIC_SDA0/DM0_DATA/GPIO21
GPIO13/TDM0_CLK/SLIMBUS_CLK/DM1_DATA
GPIO15/TDM0_RXD/SLIMBUS_DATA/UART1_RXD
MIP_IP
MIC_IN
VREF
GPIO0/DM1_CLK/TDM1_TXD_BYPASS/STRAP_TEST
GPIO19/DM0_CLK/TDM1_CLK/TDM0_CLK_BYPASS
GPIO20/DM0_DATA/TDM1_RXD
GPIO16/TDM0_TXD/TDM1_RXD_BYPASS/STRAP0
GPIO8/DM0_CLK/UART1_TXD/RTCK/JTAG_EN
GPIO9/IIC_SCL2/UART1_RXD/DM0_DATA/TDI
GPIO10/IIC_SDA2/TDM1_FSYNC/TDM0_FSYNC_BP
GNDA
VSS
U1103
DSP_DBMD4
C1133 1.0uF
C1134 1.0uF
C1135 1.0uF
DBM_IN3_P [11]
DBM_INT3_M [11]
NC TP35 NC TP36
DCDC_SY8842
NOTE: L1101 2016, 0.8mm
1.1V always on
[5,6,7,8,9,10,11,16,18] VPH_PWR
[3] DBMD_DVDD_EN
IN
PG
EN
GND
LX
OUT
FB
U1102
L1101 0.68uH
C1106 10uF
R1107 0201 100K_NC
R1103 0201 100K
R1101 0201 100K_1%
R1102 0201 120K_1%
C1110 NC
C1107 10uF
C1155 10uF
DBMD_DVDD_1.1 [11]
VOUT=0.6V¡Á (1+RH/RL)
Earphone Audio
Note: Ferrite beads and their corresponding bypass capacitors on
on CDC_HPH_L_P, CDC_HPH_L_M and CDC_HPH_REF
are needed to reduce noise generated by audio/FM concurrency
nokia,L-R-MIC-GND
default Iphone,L-R-GND-MIC
[9] MIC_BIAS2
R1105 0201 2.2K
[9,13] CDC_HPH_R
[9,13] CDC_HPH_REF
[9,13] CDC_HPH_L
[9] CDC_MIC2_P
C1140 33pF
HPH_R
HPH_L
MIC_IN
R1106 0201 0R
HEADSET_MIC_P_S [13]
[3,13] AUDIO_SEL
VREG_L13A_1P8
IN1
GND
IN0
IN2
VCC
Y
U1104
GATE_SN74LVC1G97DSF
[6,13] USB_CC1
R1108 0201 100k
C1105 NC
C1142 100nF
CDC_HS_DET [9]
REVISION RECORD
LTR
ECO NO:
APPROVED:
DATE:
COMPANY: <Company Name>
TITLE: <Title>
DRAWN: <Drawn By>
DATED: <Drawn Date>
CHECKED: <Checked By>
DATED: <Checked Date>
QUALITY CONTROL: <QC By>
DATED: <QC Date>
RELEASED: <Released By>
DATED: <Release Date>
CODE: <Code>
SIZE: A0
DRAWING NO: <Drawing Number>
REV: <Revision>
SCALE:
CAD NOTE: VIA DIRECTLY TO MAIN GND. DON'T CONNECT TO ANY OTHER GND
SHEET 11 OF 22

REVISION RECORD			
LTR	ECO NO	APPROVED	DATE

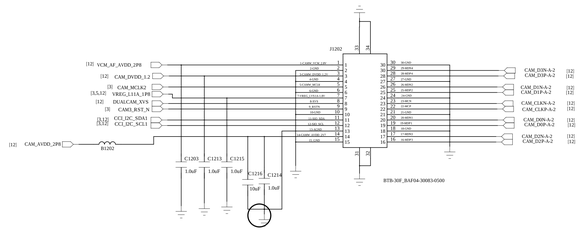
Main Camera A

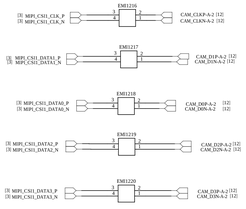




Module	Sensor IC	DOVDD	DVDD	AVDD	AFVDD
	IMX376-AAH5-C	1.8V	1.05V	2.8V	0W0763 140mAMax

Main Camera B

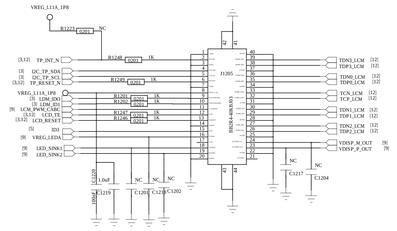


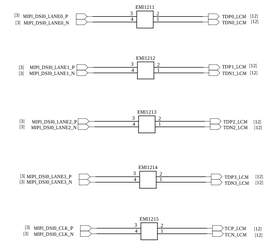


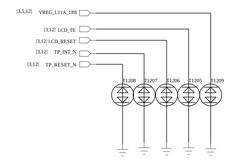
Module	Sensor IC	DOVDD	DVDD	AVDD	AFVDD
	IMX481PQHS-C	1.8V	1.2V	2.7V/2.9V	0W0763 140mAMax

LCM

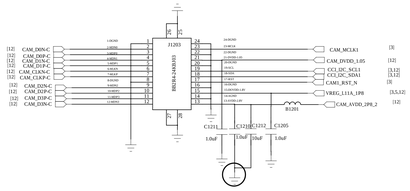
ID3 for BL LED thermal detect

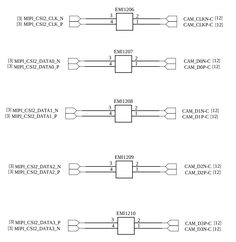






Front Camera





Module	Sensor IC	DOVDD	DVDD	AVDD	AFVDD
OLF0692(ET9)	IMX376-AAH5-C	1.8V	1.05V	2.8V	

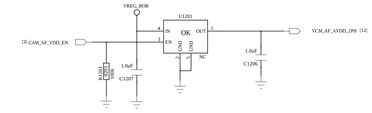
Schematic design notice of "63_PERI_CAMERA_KEYPAD" page.

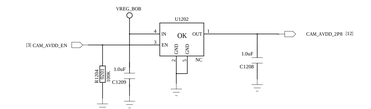
Note 62-1: The VCC of I2C_0 is pulled to "VCAM_IO_PMU".

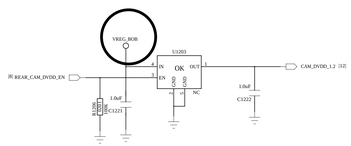
Note 62-2: I2C control interface of front camera (with AF) must be assigned to I2C-2 bus when PIP/VIV feature be supported.

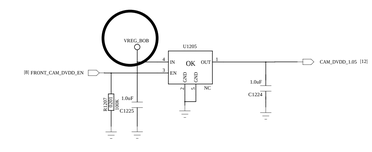
Note 62-3: Reserve a capacitor (27pF) on camera's MCLK and shunt it to GND to prevent GPS de-sense.

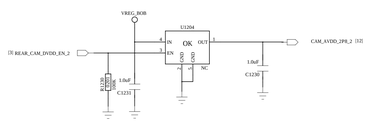
Camera Power

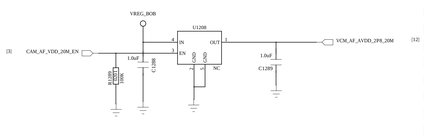




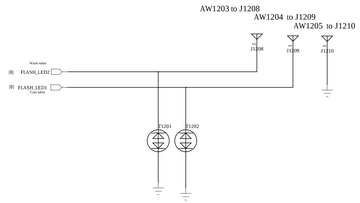


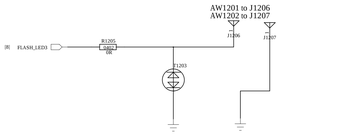






Flash Light





DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>				
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>				
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number><Revision>		REV:
RELEASED: <Released By>	DATED: <Release Date>	SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND				

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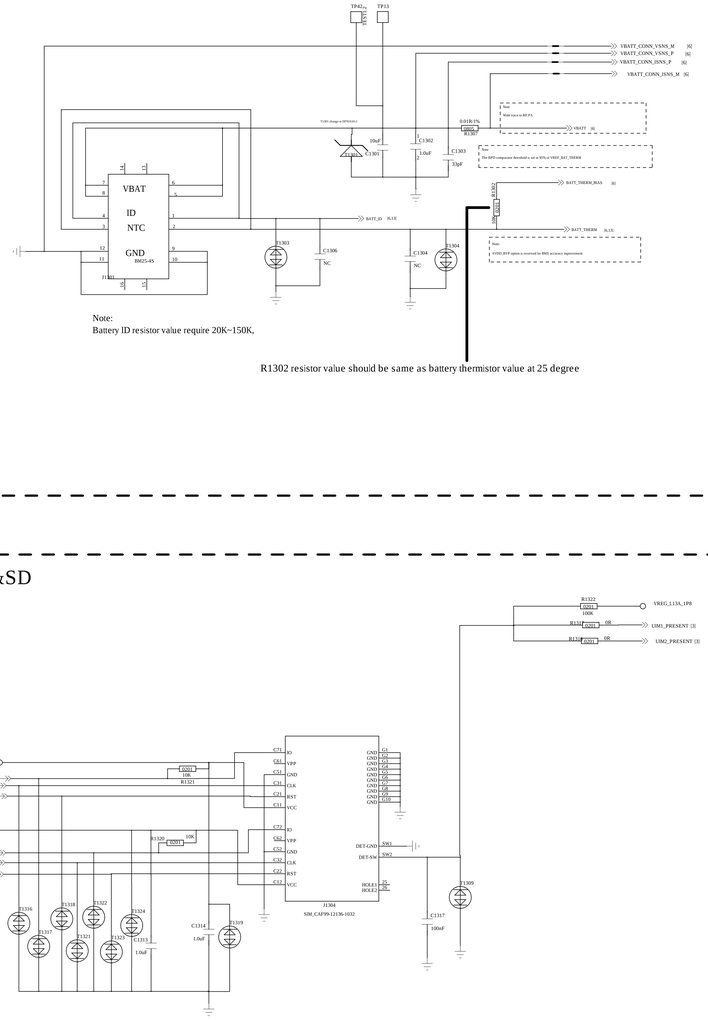
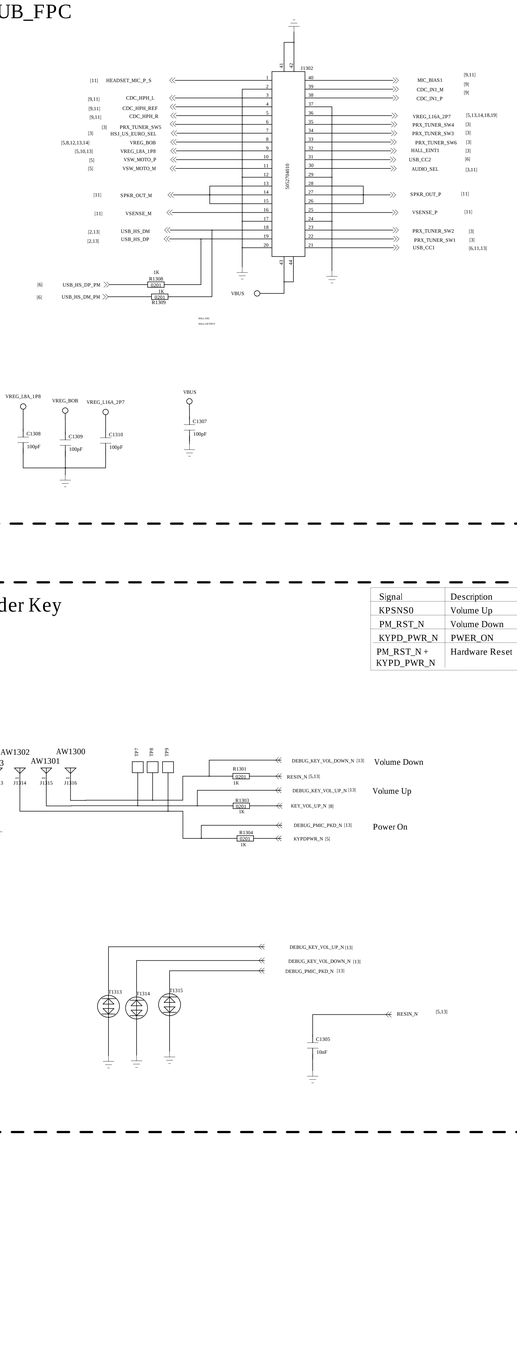
LTR	ECO NO.	APPROVED:	DATE:

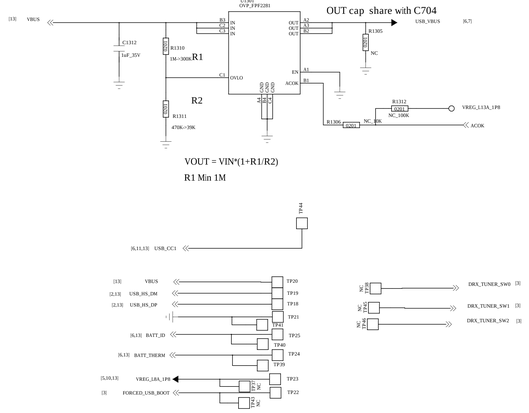
Battery Connector



SUB_FPC



OVP

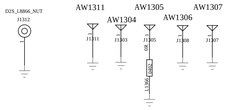


SIM&SD

Sider Key

Signal	Description
KPSNS0	Volume Up
PM_RST_N	Volume Down
KYPD_PWR_N	PWER_ON
PM_RST_N + KYPD_PWR_N	Hardware Reset

SUB_LED



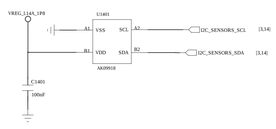
COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>		
QUALITY CONTROL: <QC By>	DATED: <QC Date>		
RELEASED: <Released By>	DATED: <Release Date>		
CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND		SHEET 2 OF 2

REVISION RECORD			
LTR	ECO NO	APPROVED	DATE

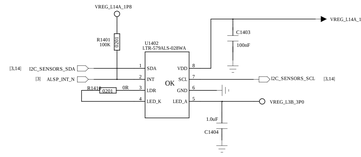
M-Sensor

M-Sensor I2C Address: 0x0C

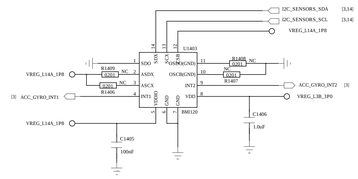
CAD	
0	0X0C
1	0X0D



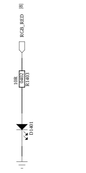
P_SENSOR

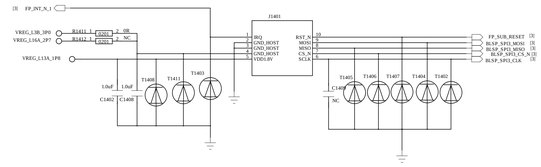


G+Gyro-Sensor



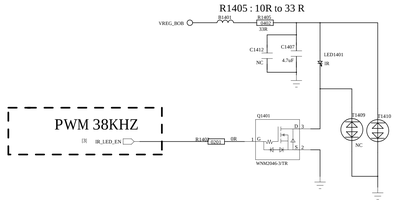
RGB





IR

R1405 : 10R to 33 R



DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>			
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>			
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DONT CONNECT TO ANY OTHER GND		

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U1501-E

SDR-660-0-180WLPSP-TR-03-0

[19]	DRX_HB1_B38_B41	141	DRX_HB1	PRX_HB1	46
[19]	DRX_HB2_B7	133	DRX_HB2	PRX_HB2	54
[19]	DRX_HB3_B40	126	DRX_HB3	PRX_HB3	63
[19]	DRX_HB4_B34	117	DRX_HB4	PRX_HB4	71
		118	DRX_UHB	PRX_UHB	80
[19]	DRX_MB1_B3	173	DRX_MB1	PRX_MB1	16
[19]	DRX_MB2_B39	164	DRX_MB2	PRX_MB2	25
[19]	DRX_MB3_B2	156	DRX_MB3	PRX_MB3	32
[19]	DRX_MB4_B1_B4	148	DRX_MB4	PRX_MB4	38
		179	DRX_LB1	PRX_LB1	7
		170	DRX_LB2	PRX_LB2	15
[19]	DRX_LB3_B20	178	DRX_LB3	PRX_LB3	6
[19]	DRX_LB4_B8	169	DRX_LB4	PRX_LB4	14
[19]	DRX_LB5_B5_B26	177	DRX_LB5	PRX_LB5	5
		101	DRX_LTEU_UHB	PRX_LTEU_UHB	86
		68	TX_FBRX_M	TX_CH0_HB1	26
[18]	TX_FBRX_P	66	TX_FBRX_P	TX_CH0_MB1	33
		161	GNSS_IN	TX_CH0_MB2	10
				TX_CH0_UMB	18
				TX_CH0_LB1	2
				TX_CH0_LB2	27
				TX_CH1_UHB	168
				TX_CH1_HB	167
				TX_CH1_MB	159
				TX_CH1_LTEU	176

PRX_HB1_B38_B41	[18]	TX_CH0_HB1_LTE_B7_B38_B40_B41	[18]
PRX_HB2_B7	[17]	TX_CH0_MB1_B1_B2_B3_B4_B34_B39	[18]
PRX_HB3_B40	[18]	TX_CH0_MB2_DCS_PCS	[18]
PRX_HB4_B34	[17]	TX_CH0_LB1_G850_G900	[18]
PRX_MB1_B3	[17]	TX_CH0_LB2_W5_W8_LTE_B5_B8_B20_B28	[18]
PRX_MB2_B39	[18]		
PRX_MB3_B2	[17]		
PRX_MB4_B1	[17]		
PRX_LB3_B20	[17]		
PRX_LB4_B8	[17]		
PRX_LB5_B5_B26	[17]		

C1537 0R 0402 — TX_FBRX_M

C1532 33pF — C1525 2.4nH — 5.1nH C1526 — [21] GPS_SDR660

U1501-C

SDR-660-0-180WLPSP-TR-03-0

Pin 108,37,107,1 Power group

VREG_L2A_1P8	VDD_ANALOG_1P8	C1505 4.7uF	
		C1504 100nF	VDDA_1P0_RX1 77
		C1502 100nF	VDDA_1P0_RX2 37
		C1503 100nF	VDDA_1P0_XO 107
			VDDA_1P0_RX2 43
			VDDA_1P0_RX 95
			VDDA_1P0_RX2_1 53
		C1551 100nF	VDDA_1P0_TX1 144
		C1552 100nF	VDDA_1P0_RX0 154
		C1553 100nF	VDDA_1P0_GNSS 146
			VDDA_1P0_RX0_1 132
		C1554 100nF	VDDA_1P0_TX0_1 13
		C1555 100nF	VDDA_1P0_TX0 3
Pin 152,121,122volte one group			VDDA_1P8_TX1 152
		C1556 100nF	VDDA_1P8_ANA2 121
		C1557 100nF	VDDA_1P8_TX0 11
			VDDA_1P8_ANA1 35
VREG_L12A_1P8	VDD_ANALOG_1P8	C1560 4.7uF	VDDA_1P8_ANA2 122
		C1558 100nF	VDDA_1P8_RX2 69
			VDDA_1P8_FBRX 50
			VDDA_1P8_FBRX 59

VDDA_1P2_RX1	108	C1559 100nF	REG_L7A_1P2
VDDA_1P2_RX2	70		
VDDA_1P2_ANA0	75		
VDDA_1P2_ANA0	90		
VDDA_1P2_FBRX	85	C1561 100nF	C1564 4.7uF
VDDA_1P2_TX0	29	C1562 100nF	
VDDA_1P2_RX0	130		
VDDA_1P2_RX0	137		
VDDA_1P2_RX0_1	123	C1563 100nF	
VDDD_1P0_QLINK	118	0R 0201 C1529	VREG_L3A_1P0
VDDD_1P0	64	C1565 100nF	C1570 4.7uF
VDDD_1P0	82	C1566 100nF	
VDDD_1P0	142		
VDDD_1P8	112	0R 0201 C1568	VREG_L13A_1P8
		C1567 100nF	C1569 4.7uF

U1501-A

SDR-660-0-180WLPSP-TR-03-0

[5]	RF_CLK2	0R 0201 C1571	XO_IN	114	
		C1502 0201	W_GRFC_6	120	
			W_GRFC_7	157	
			W_GRFC_5	136	
			DNC_2	165	
[3]	QLINK_ENABLE	GPIO100	QLINK_EN	143	
[3]	QLINK_REQUEST	GPIO99	QLINK_REQ	73	
[21]	GNSS_ELNA_CTRL		GNSS_ELNA_CTRL	150	
			DNC_1	66	
			RFFE1_CLK	166	RFFE1_CLK [3]
			RFFE1_DATA	149	RFFE1_DATA [3]
			DNC_3	173	
WMSS_RESETN		GPIO78	WMSS_RESETN	83	WMSS_RESETN [3]
			W_GRFC_0	57	
			W_GRFC_1	85	
			W_GRFC_2	74	

U1501-D

SDR-660-0-180WLPSP-TR-03-0

	1	GND_1	
	9	GND_4	
	115	GND_50	
	124	GND_52	
	106	GND_48	
	91	GND_38	
QLINK_CLK_M	81		QLINK_CLK_M [3]
QLINK_CLK_P	96		QLINK_CLK_P [3]
QLINK_TX_M	87		QLINK_TX_M [3]
QLINK_TX_P	72		QLINK_TX_P [3]
QLINK_RX0_M	88		QLINK_RX0_M [3]
QLINK_RX0_P	103		QLINK_RX0_P [3]
QLINK_RX1_M	111		QLINK_RX1_M [3]
QLINK_RX1_P	127		QLINK_RX1_P [3]
QLINK_RX2_M	135		QLINK_RX2_M [3]
QLINK_RX2_P	119		QLINK_RX2_P [3]
ETDAC_CH0_M	47		
ETDAC_CH0_P	39		
ETDAC_CH1_M	113		
ETDAC_CH1_P	104		

U1501-B

SDR-660-0-180WLPSP-TR-03-0

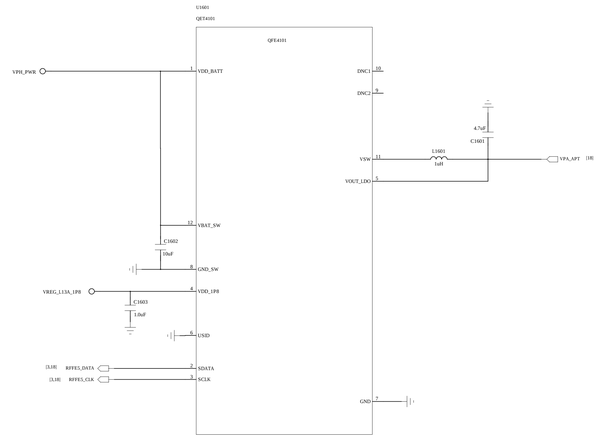
	99	GND_44	
	45	GND_24	
	58	GND_29	
	67	GND_32	
	84	GND_36	
	98	GND_43	
	89	GND_37	
	150	GND_66	
	138	GND_58	
	116	GND_51	
	61	GND_30	
	34	GND_16	
	40	GND_18	
	129	GND_55	
	105	GND_47	
	109	GND_49	
	125	GND_53	
	140	GND_60	
	155	GND_65	
	163	GND_69	
	172	GND_70	
	12	GND_5	
	19	GND_7	
	48	GND_23	
	28	GND_13	
	20	GND_8	
	175	GND_72	
	160	GND_67	
	153	GND_64	
	100	GND_45	
	4	GND_2	
	174	GND_71	
	55	GND_27	
	180	GND_73	
	8	GND_3	
GND_19	41		
GND_9	23		
GND_10	22		
GND_17	36		
GND_20	42		
GND_28	56		
GND_42	97		
GND_54	128		
GND_57	134		
GND_56	131		
GND_59	139		
GND_39	92		
GND_14	30		
GND_35	79		
GND_31	62		
GND_22	45		
GND_15	31		
GND_12	24		
GND_6	17		
GND_11	23		
GND_61	145		
GND_63	151		
GND_25	51		
GND_33	76		
GND_26	52		
GND_62	147		
GND_68	162		
GND_34	78		
GND_40	93		
GND_21	44		
GND_41	94		
GND_46	102		

Each QPHY pair shall be routed in a channel together isolated from other QPHY pairs with surrounding gnd

QPHY_ETDAC_TEST

COMPANY:	<Company Name>		
TITLE:	<Title>		
DRAWN: <Drawn By>	DATED: <Drawn Date>		
CHECKED: <Checked By>	DATED: <Checked Date>	CODE: <Code>	SIZE: A0
QUALITY CONTROL: <QC By>	DATED: <QC Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND

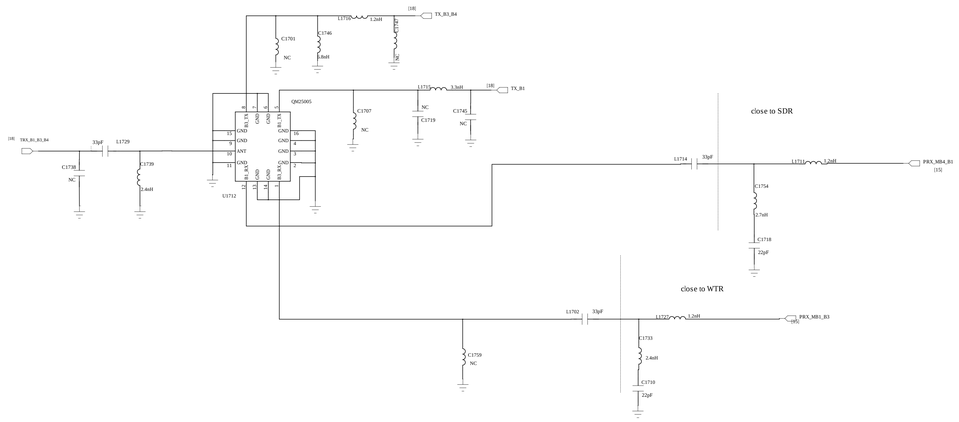
REVISION RECORD			
LTR	ECO NO	APPROVED	DATE



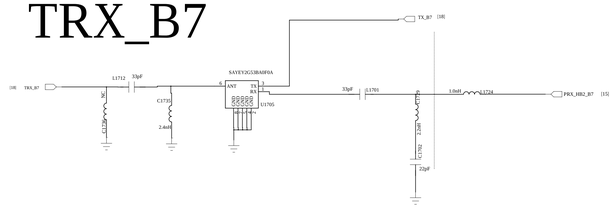
DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>			
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>			
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND			

REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:

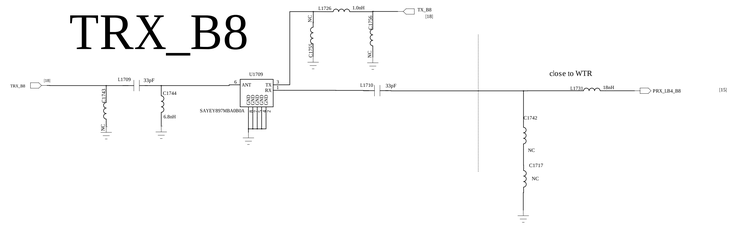
TRX_B1_B3_B4



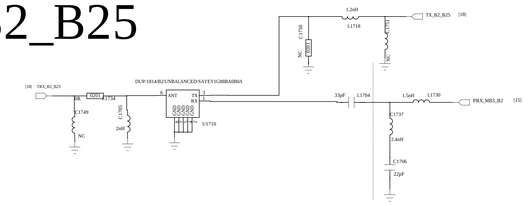
TRX_B7



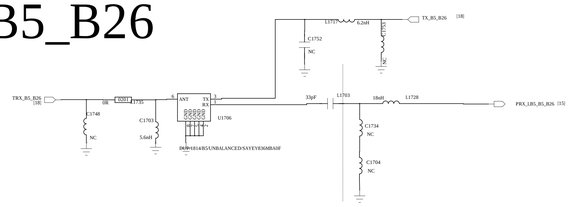
TRX_B8



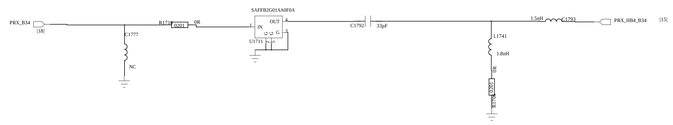
TRX_B2_B25



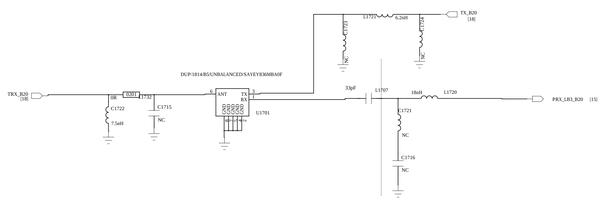
TRX_B5_B26



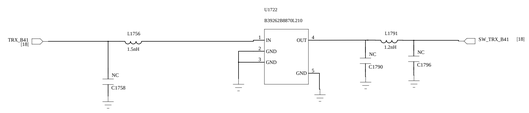
PRX_B34



TRX_B12/17_B20



TRX_B41_120M



DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO.: <Drawing Number>	REV: <Revision>
		SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND	SHEET 1 OF 1

REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:

DPDT

PRX_B41

PRX_B40

TX_B7

TRX_B40

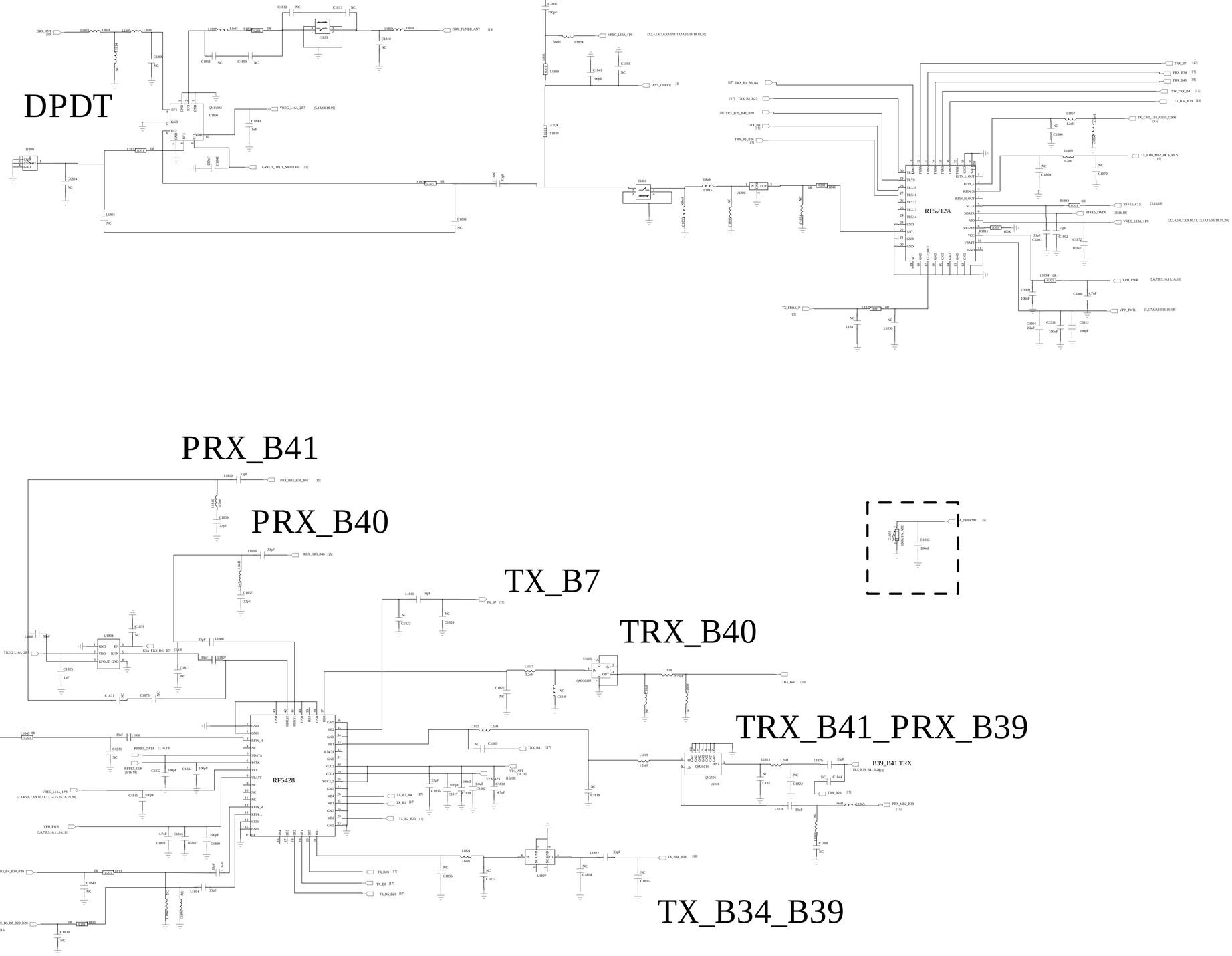
TRX_B41_PRX_B39

TX_B34_B39

RF5428

RF5212A

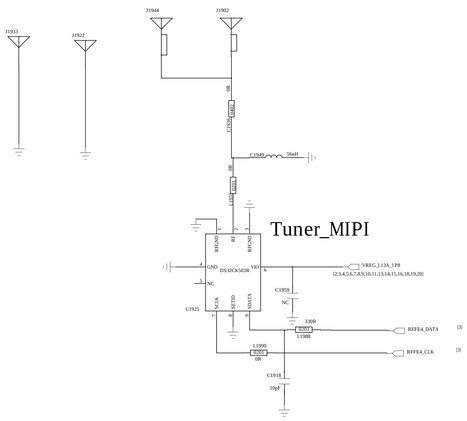
B39_B41 TRX



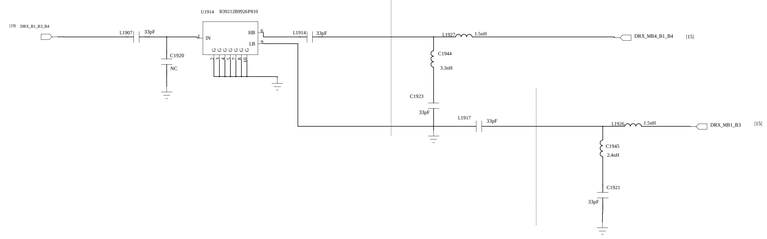
DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO.: <Drawing Number>	REV: <Revision>
		SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND	SHEET 1 OF 1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

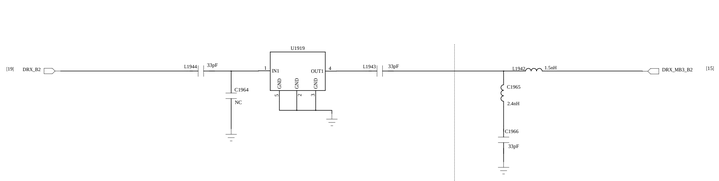
Tuner_MIPI



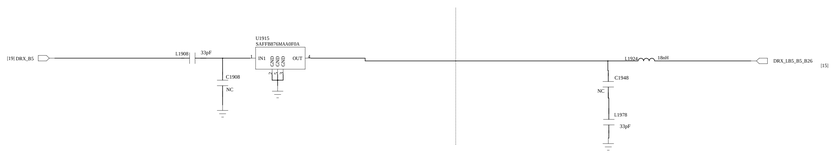
B1_B3_B4_DRX



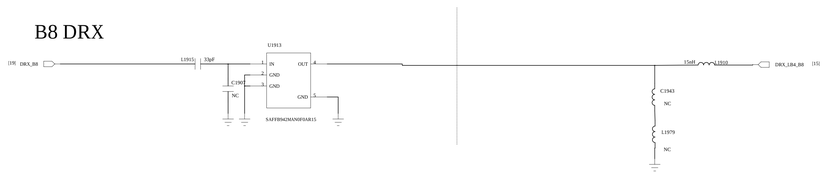
B2_DRX



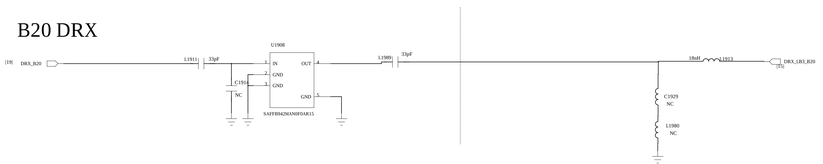
B5_DRX



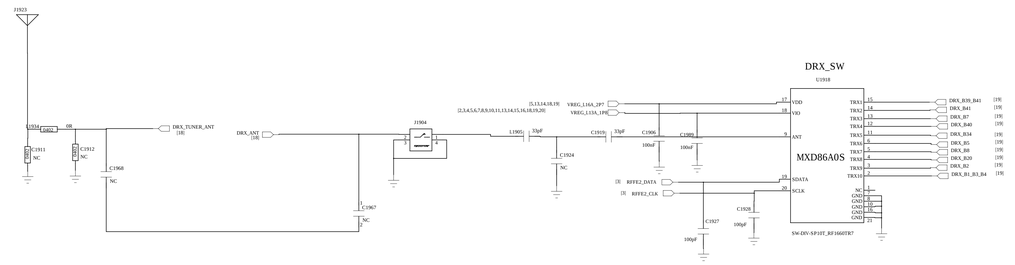
B8 DRX



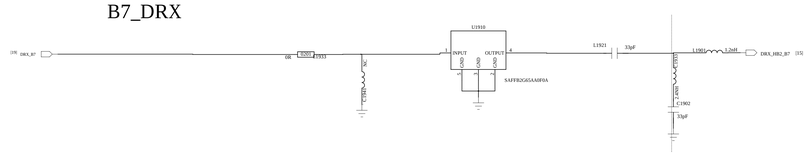
B20 DRX



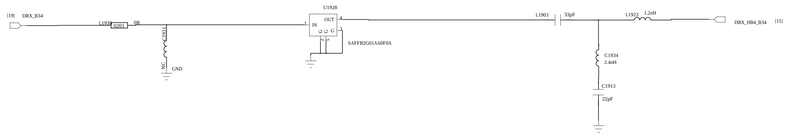
DRX_SW



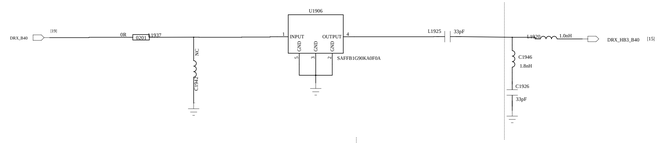
B7_DRX



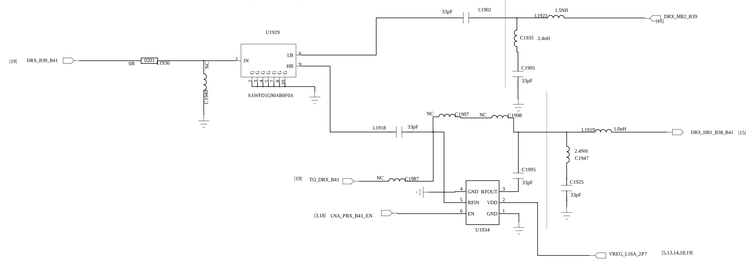
DRX_B34



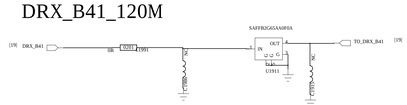
B40_DRX



B39_B41_DRX



DRX_B41_120M



DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number>	REV: <Revision>
		SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND	SHEET 1 OF 1

REVISION RECORD			
LTR	ECO NO	APPROVED	DATE

U2001-A

WCN-3980-0-828WLP5P-TR-0B-0

WCN3980

[3]	WL_BB_IP_RX	53	WL_BB_IP_RX		
[3]	WL_BB_IN_TX	73	WL_BB_IN_TX		
[3]	WL_BB_IP_TX	80	WL_BB_IP_TX		
[3]	WL_BB_QN_RX	59	WL_BB_QN_RX		
[3]	WL_BB_QP_RX	52	WL_BB_QP_RX		
	WL_RF_PDET_IN	27	WL_RF_PDET_IN_CH0		
[21]	WL_BT_RFIO_2G_CH0	42	WL_BT_RFIO_2G_CH0		
[3]	WL_BB_QP_TX	79	WL_BB_QP_TX		
[3]	WL_BB_IN_RX	60	WL_BB_IN_RX		
	WL_RFI_5G_CH0	75	WL_RFI_5G_CH0	[21]	WL_RFI_5G_CH0
	WP_P	10	0R C2036 0.5pF		
	WL_RFO_5G_CH0	68	WL_RFO_5G_CH0	[21]	WL_RFO_5G_CH0
	LF_CLK_IN	36	SLEEP_CLK	[2,5]	
	CLK_OUT	65	C2005 22pF, 0R, C2006 56pF, 0R, C2027		WLAN_5G_CLK_OUT [3]
	WL_CMD_DATA_CH0	17	0R R2027 C2028		WL_CMD_DATA_CH0 [3]
	WL_CMD_CLK_CH0	9	0R R2021 C2029		WL_CMD_CLK_CH0 [3]
	XTALI	44			XTALI [20]
	XTALO	37			
	WL_BB_QN_TX	72			WL_BB_QN_TX [3]
	FM_RX_HEADSET	7			

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WCN3980

	SENS_TXD	3	SENS_TXD	[3]	SDM/CHC_CI
	SENS_RXD	23	SENS_RXD	[3]	SDM/CHC_CI
	COEX_TXD	70	COEX_TXD	[3]	SDM/GPIO82
	COEX_RXD	57	COEX_RXD	[3]	SDM/GPIO83
[3]	CTS	64			SDM/GPIO59
	WL_BT_FEM_0	31			
	WL_BT_FEM_3	25			
	WL_BT_FEM_2	11			
[21]	LNA_EN_5G_CH0	39	WL_BT_FEM_1		
	GP_EN	40			
	GP_IN	14			
	WL_BT_FEM_4	45			
	GP_OUT	13			
[21]	PA_EN_5G_CH0	58	WL_BT_FEM_5		
	SW_CTRL	15	WLAN_SW_CTRL	[5,8]	SDM/GPIO5
	RXD	16	RXD	[3]	SDM/GPIO56
	RTS	50	RTS	[3]	SDM/GPIO58
	TXD	8	TXD	[3]	SDM/GPIO57
	SB_CLK	22	SB_CLK	[3]	
	SB_DATA	63	SB_DATA	[3]	
	COEX_CLK	76	COEX_CLK	[3]	
	COEX_DATA	77	COEX_DATA	[3]	

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WCN3980

	GND_WL_5G_DRV_CH0	74		
	GND_FM_VCO	20		
	GND_FM_RXFE	6		
	GND_WL_SYNTH_CH0	51		
	GND_WL_5G_PA_CH0	67		
	GND_WL_BALUN_CH0	62		
	GND_WL_2G_PA_CH0	54		
	GND_WL_BT_DRV_VH0	48		
	GND_WL_BT_RXFE_CH0	35		
	GND_DIG	30		
	GND_ISO	24		
	GND_BT_FM_BBPLL_A	18		
	GND_GP	21		
	GND_IO	49		
	GND_XTAL	38		
	GND_PM	65		
	GND_PDET	28		
	GND_DPD_CH0	41		
	GND_BT_SYNTH	19		
	GND_WL_5G_RXFE_CH0	61		
	GND_WL_BB_CH0	66		
	VDD33_PM_DLDO	23	VREG_L19A_3P3	[5,20]
	VDD33_WL_5G_DRV_CH0	63	VREG_L19A_3P3	[5,20]
	GND_ESD_0	47		
	VDD33_WL_CH0	55	VREG_L19A_3P3	[5,20]
	GND_SEALRING3	78		
	VDD18_IO	56	VREG_L13A_1P8	[2,3,4,5,6,7,8,9,10,11,13,14,15,16,18,19,20]
	VDD13_FM	12	VREG_L6A_1P3	[4,5,20]
	VDD13_BT_BB_WL	26	VREG_L6A_1P3	[4,5,20]
	VDD13_BT_FM_BBPLL	4	VREG_L6A_1P3	[4,5,20]
	VDD33_WL_BT_DRV_CH0	34	VREG_L19A_3P3	[5,20]
	VDD33_FEM	2	VREG_L19A_3P3	[5,20]
	GND_SEALRING1	82		
	GND_BT_BB	33		
	VDD11D_PM	43	VDD11D_PM	[20]
	VDD13_PM	29	VREG_L6A_1P3	[4,5,20]
	GND_SEALRING2	1		
	VDD13_WL_SYNTH_CH0	46	VDD13_WL_SYNTH_CH0	[20]
	VDD13_BT_SYNTH	5	VREG_L6A_1P3	[4,5,20]
	VDD18_XTAL	32	VREG_L9A_1P8	[4,5,20]

XTALI [20]

C2007 100pF

RF_CLK1 [5]

1.3V_RFA

VREG_L6A_1P3 [4,5,20]

0R R2023 C2026 10nF C2005

C2023 4.7uF

VDD13_WL_SYNTH_CH0 [20] Pin 46

VREG_L6A_1P3 [4,5,20]	C2022 10nF	Pin 5
VREG_L6A_1P3 [4,5,20]	C2008 10nF	Pin 29
VREG_L6A_1P3 [4,5,20]	C2014 10nF	Pin12
VREG_L6A_1P3 [4,5,20]		Pin 4
VREG_L6A_1P3 [4,5,20]	C2024 10nF	Pin 26

3.3V CH0

VREG_L19A_3P3 [5,20]

12,17 C2012 10nF

VREG_L19A_3P3 [5,20]	C2002 4.7uF, C2019 10nF	Pin 55
VREG_L19A_3P3 [5,20]	C2013 10nF	Pin 34
VREG_L19A_3P3 [5,20]	C2021 1.0uF, C2045 100pF	Pin 61
VREG_L19A_3P3 [5,20]	C2010 10nF, C2046 100pF	Pin 71
VREG_L19A_3P3 [5,20]	C2016 10nF	Pin 2

1.8V IO

[2,3,4,5,6,7,8,9,10,11,13,14,15,16,18,19,20] VREG_L13A_1P8

C2011 4.7uF, C2015 470nF

VDD18_IO

Pin 94

1.8V XO

[10] VREG_L9A_1P8 [4,5,20]

C2017 2.2uF, C2018 470nF

VDD18_XTAL

Pin 40

1.1V

VDD11D_PM [20]

C2001 1.0uF, C2020 1.0uF

COMPANY:	<Company Name>				
TITLE:	<Title>				
DRAWN: <Drawn By>	DATED: <Drawn Date>	CODE: <Code>	SIZE: A0	DRAWING NO: <Drawing Number>	REV: <Revision>
CHECKED: <Checked By>	DATED: <Checked Date>				
QUALITY CONTROL: <QC By>	DATED: <QC Date>				
RELEASED: <Released By>	DATED: <Release Date>				

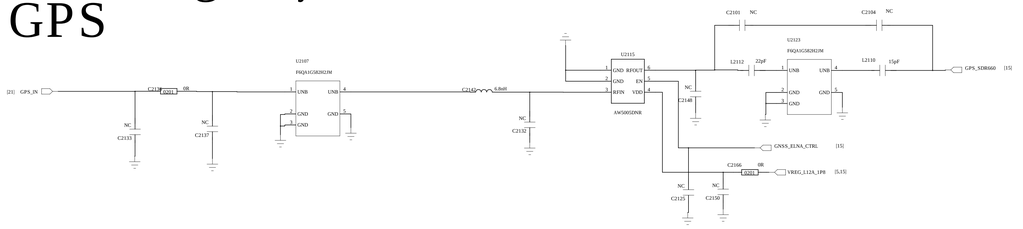
SCALE: CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND

DO NOT SCALE DRAWING

REVISION RECORD			
LTR	ECO NO.	APPROVED:	DATE:

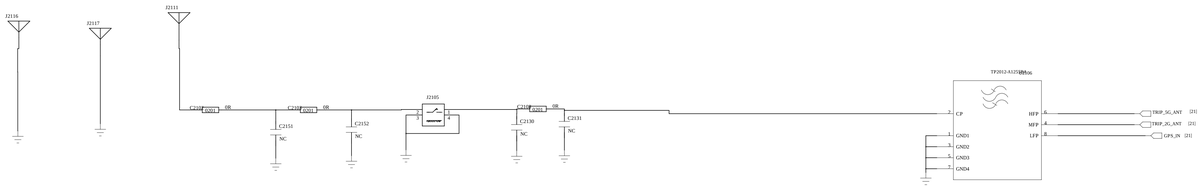
GPS

High rejection saw

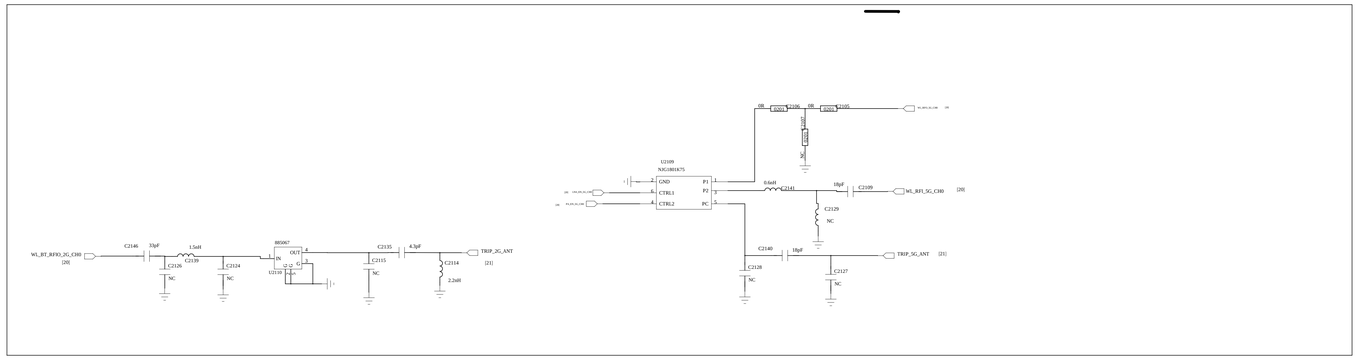


used for connect to ground

GPS_2G_5G_ANT



2G_5G_WLAN_FEM

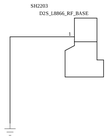


DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>	
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>	
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A0
RELEASED: <Released By>	DATED: <Release Date>	DRAWING NO: <Drawing Number><Revision>	REV:
		SCALE:	CAD NOTE: VIA DIRECTLY TO MAIN GND. DO NOT CONNECT TO ANY OTHER GND

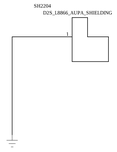
SH2201
DZS_L8866_BB_CPU_BASE

SH2202
DZS_L8866_RFPMU_SHIELDING

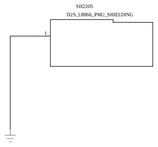
SH2203
DZS_L8866_RF_BASE



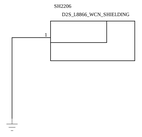
SH2204
DZS_L8866_AUPA_SHIELDING



SH2205
DZS_L8866_PMU_SHIELDING



SH2206
DZS_L8866_WCN_SHIELDING



SH2207
DZS_L8866_SMB_SHIELDING

SH2208
DZS_L8866_APT_SHIELDING