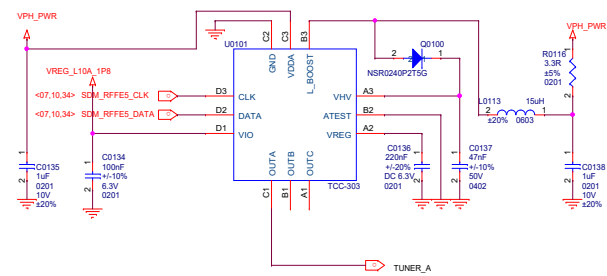
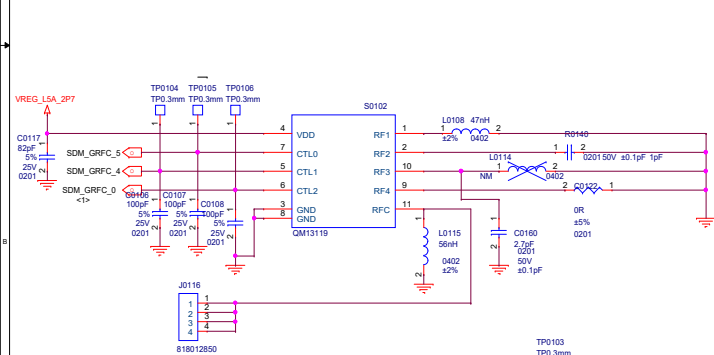
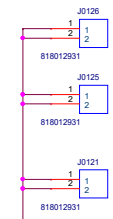
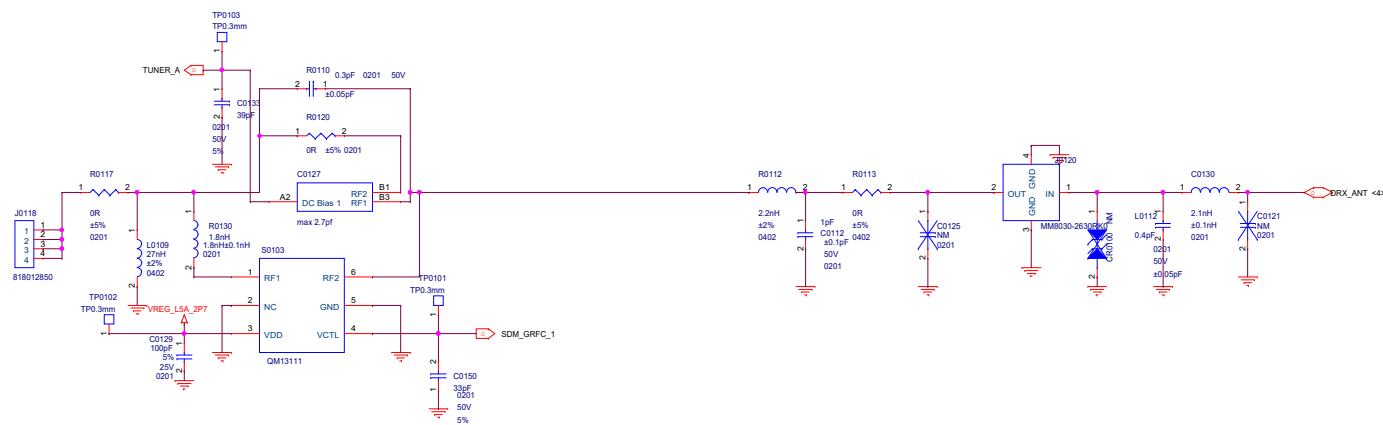


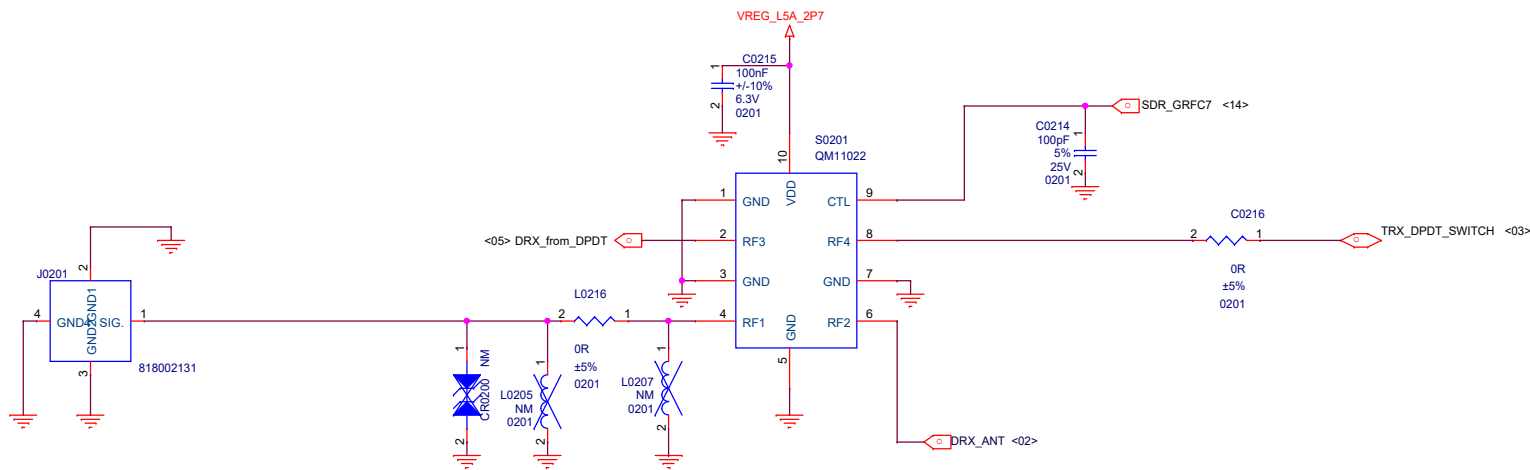
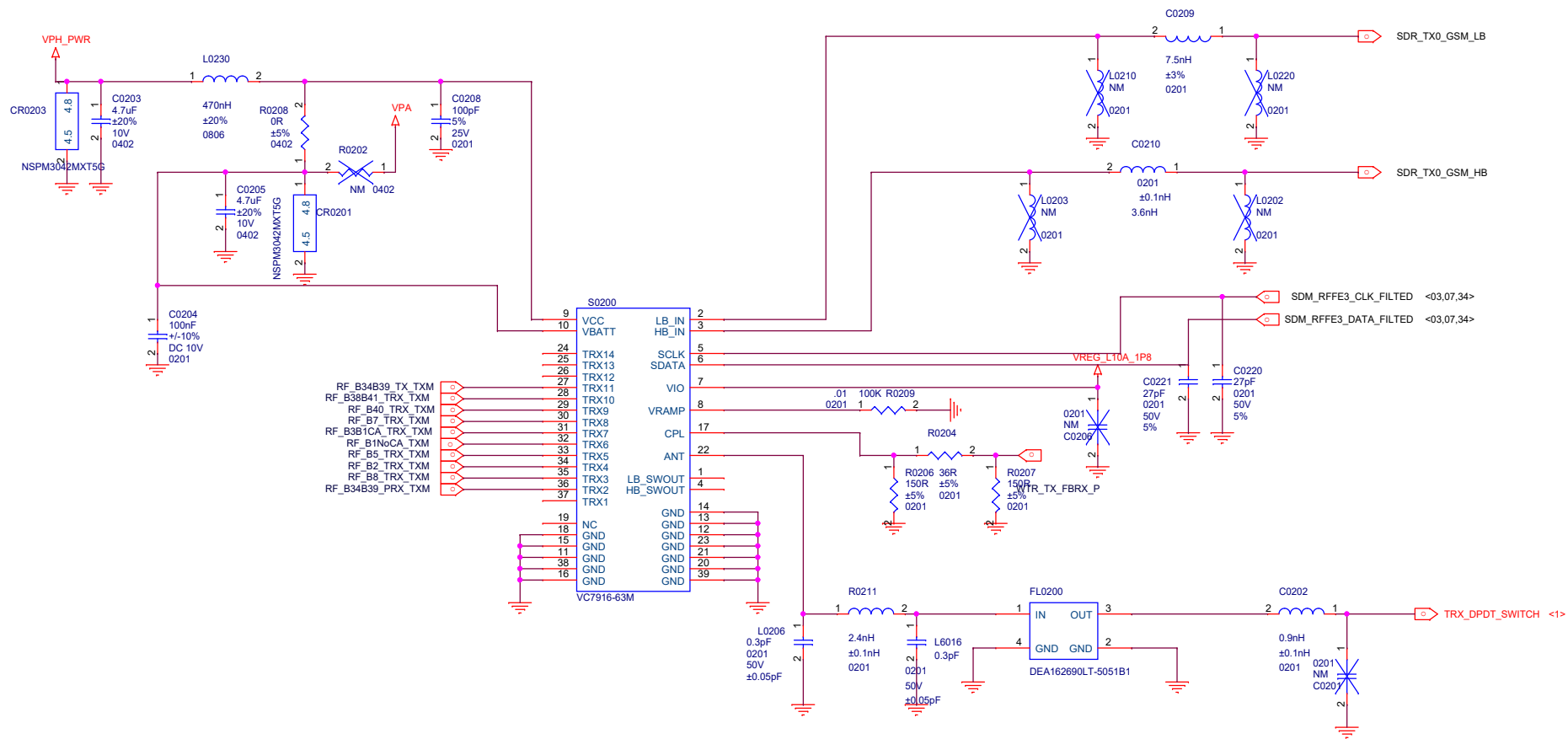
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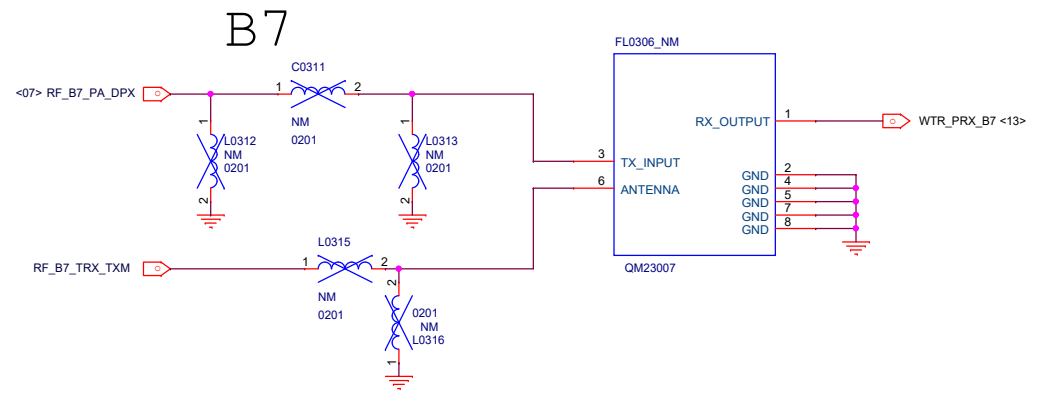
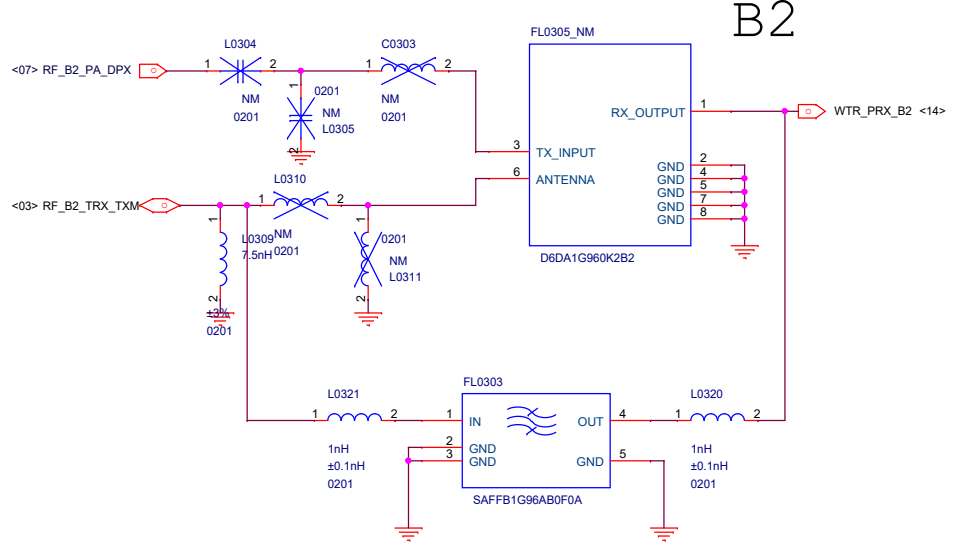
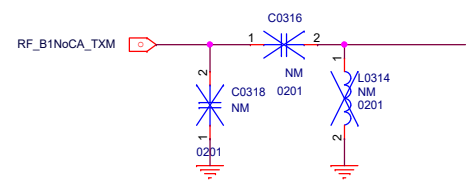
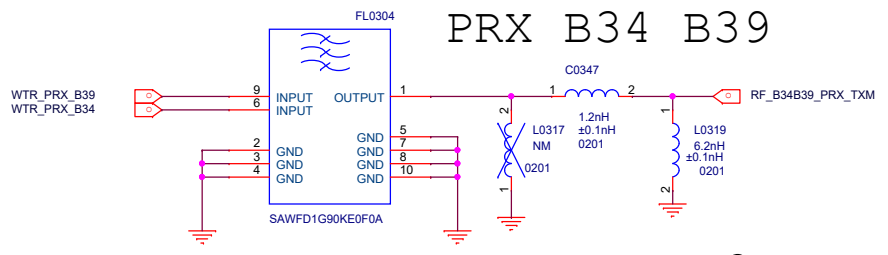
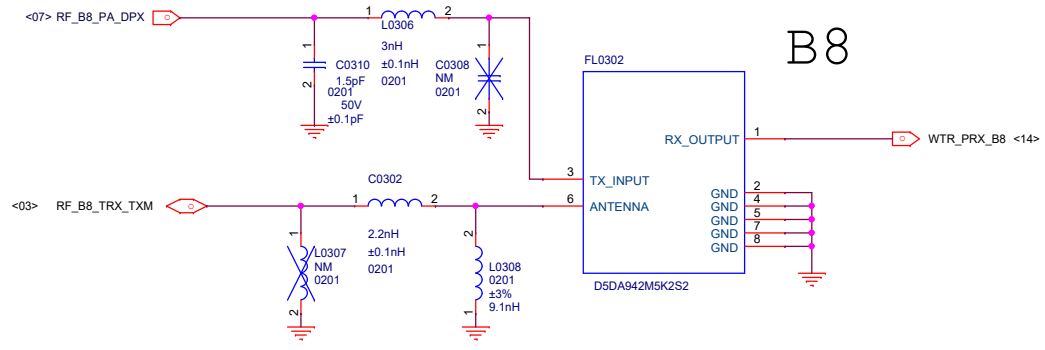
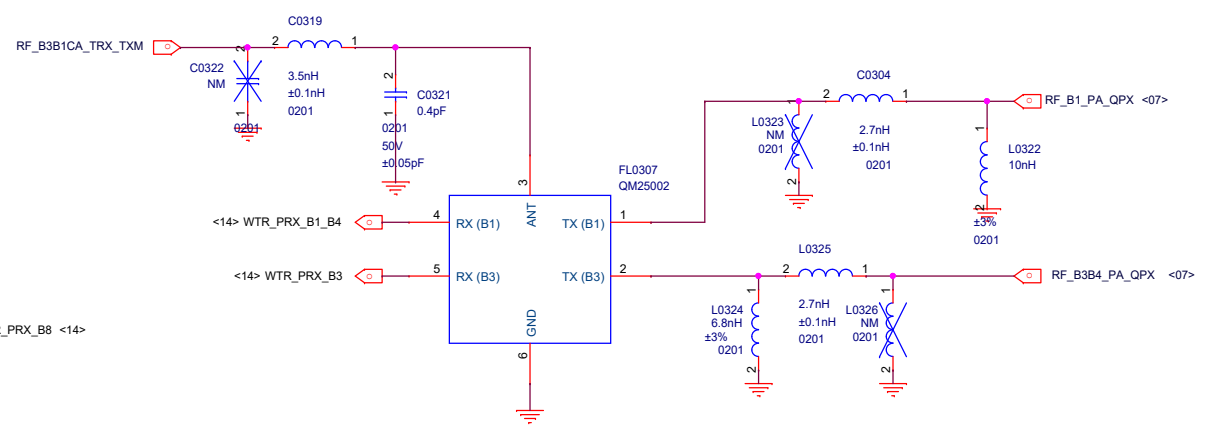
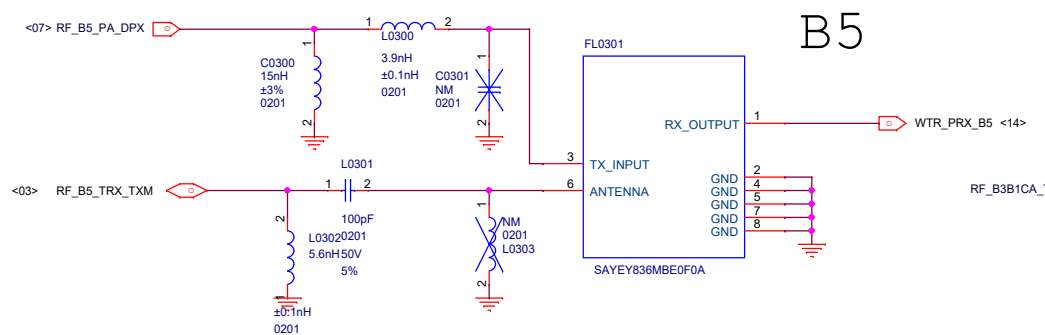
TUNER\_CTR

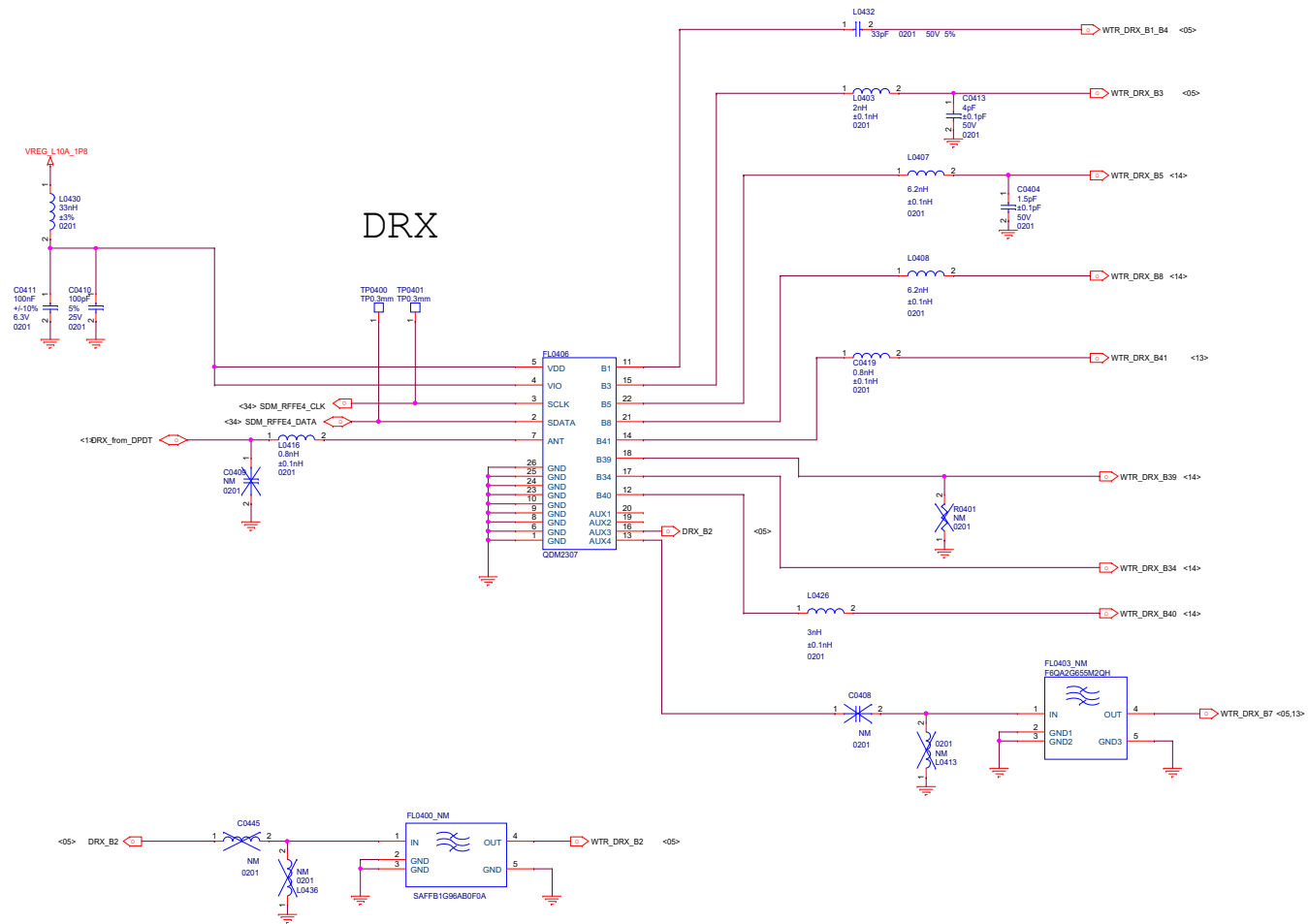


DRX\_ANT

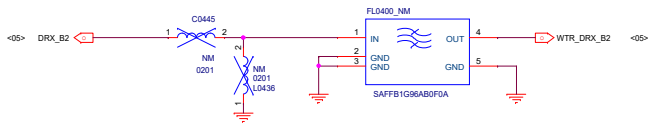








DRX



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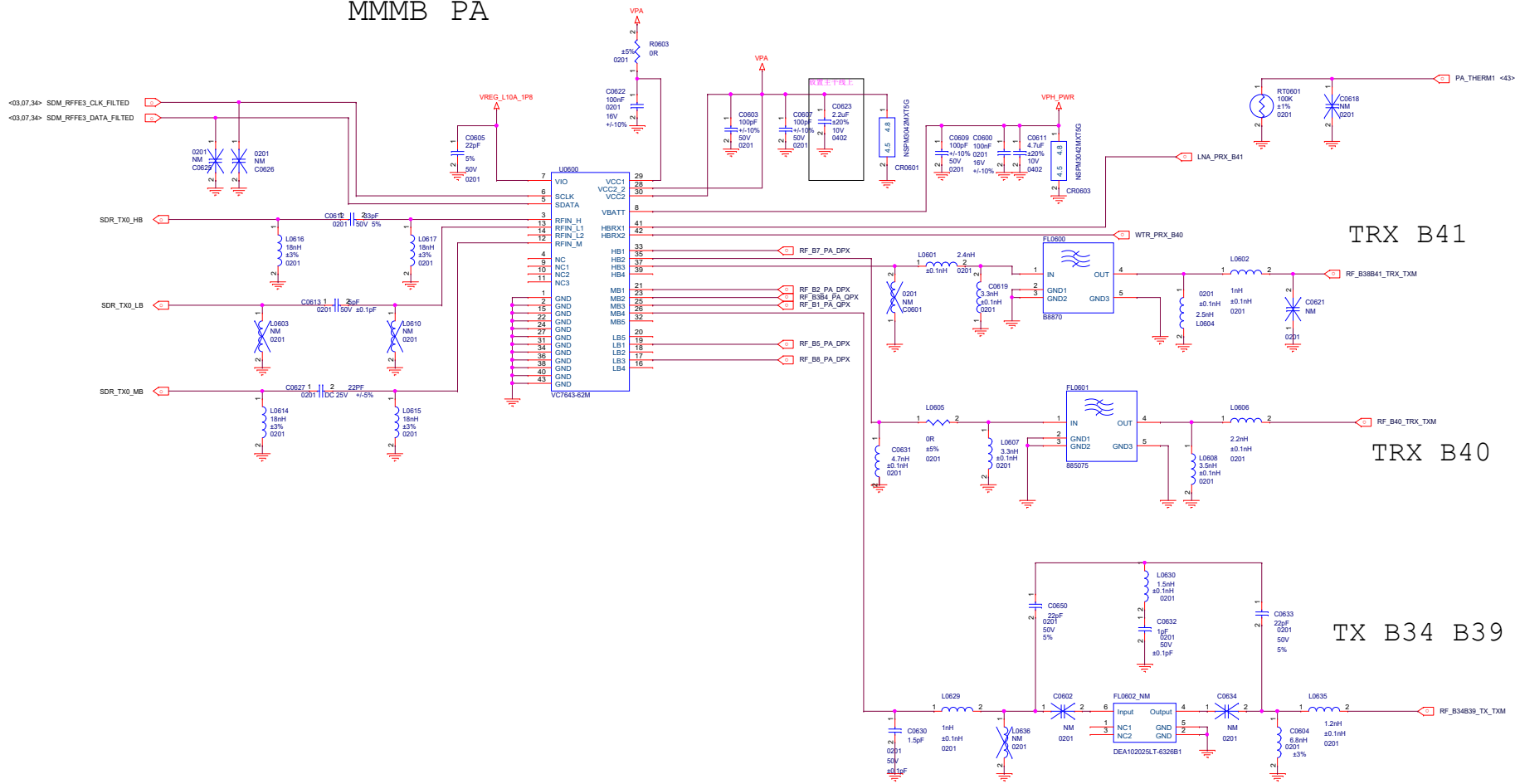
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# MMMB PA



TRX B41

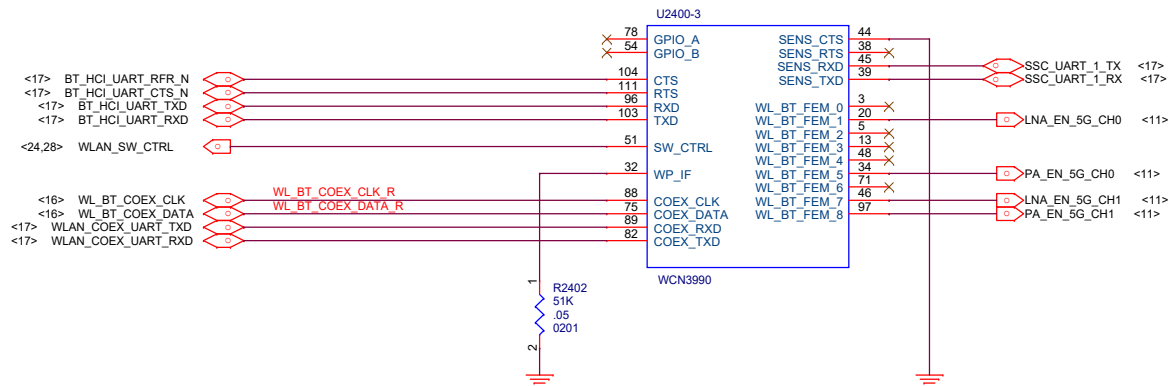
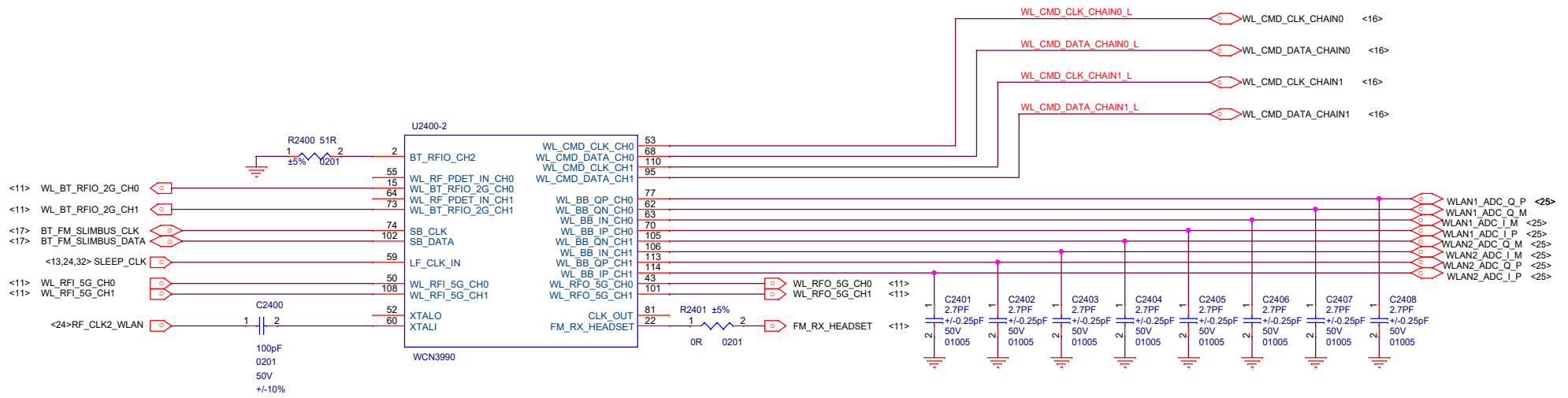
TRX B40

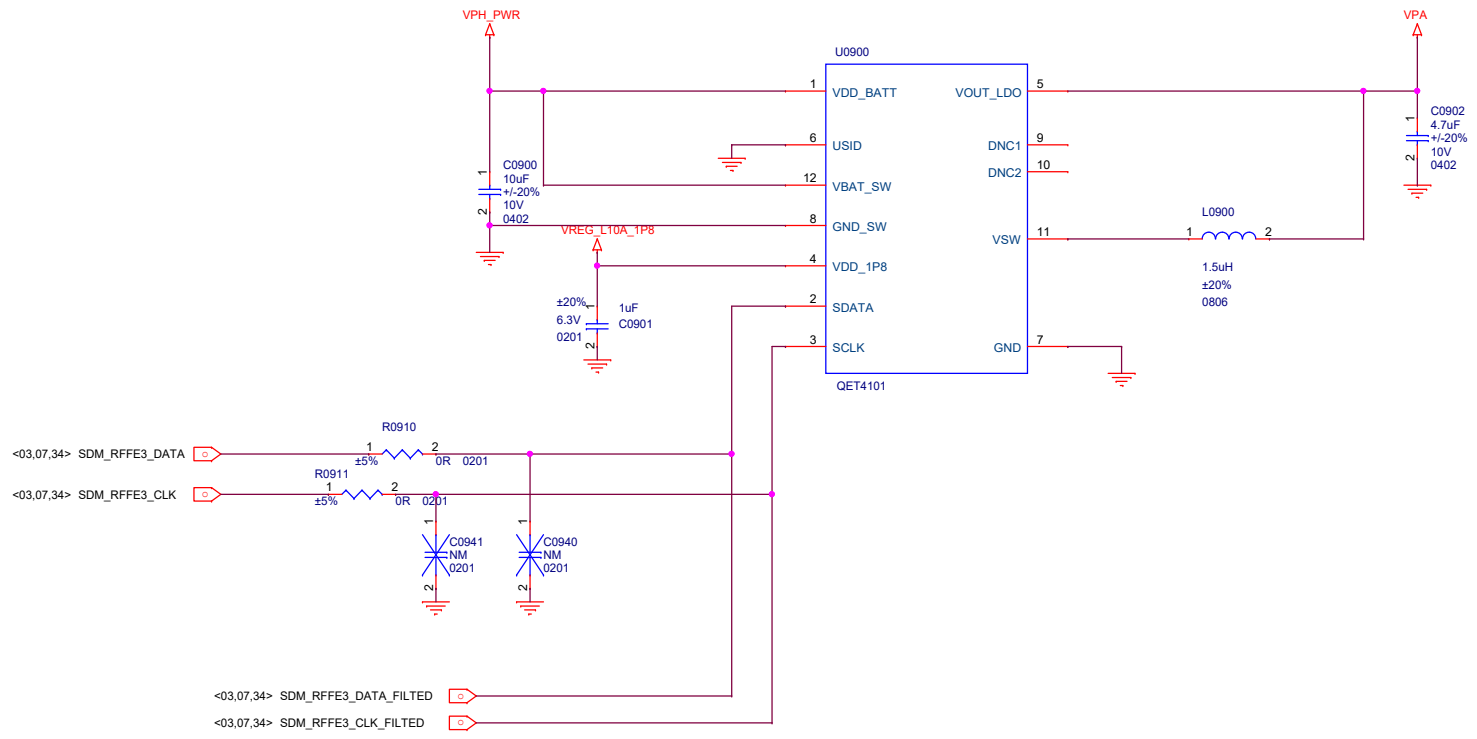
TX B34 B39





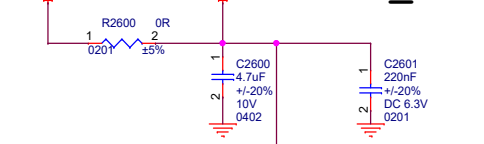




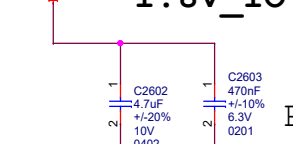




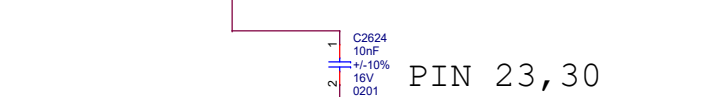
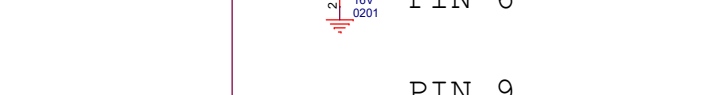
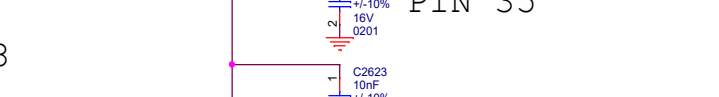
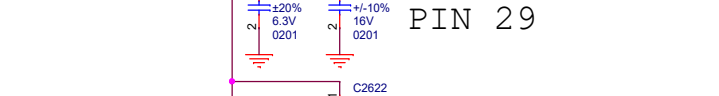
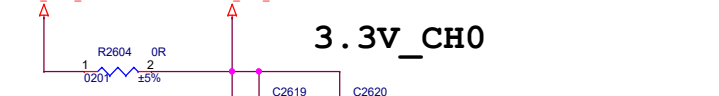
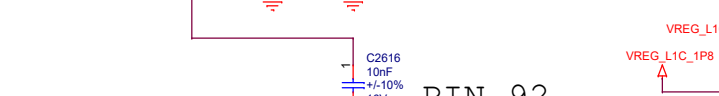
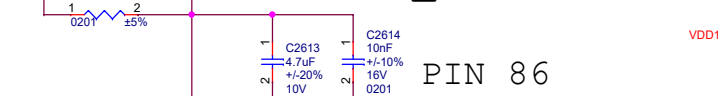
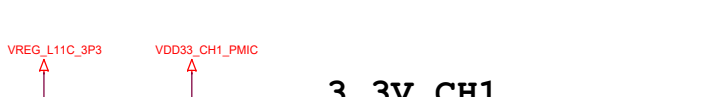
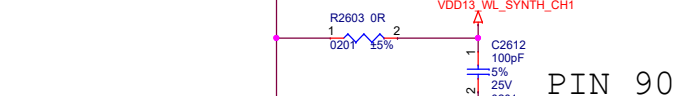
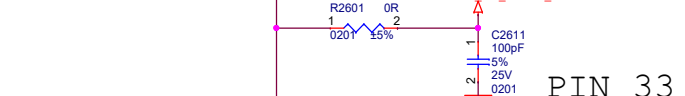
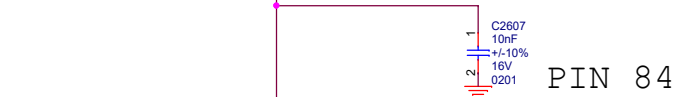
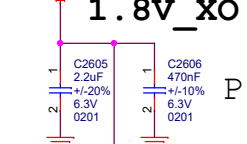
**1.3V\_RFA**



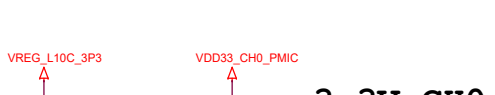
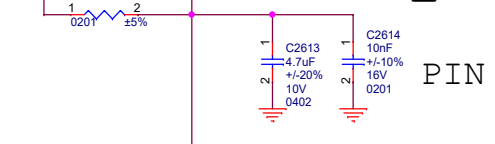
**1.8V\_IO**



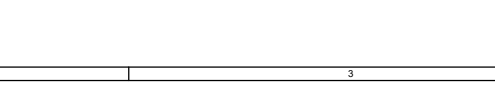
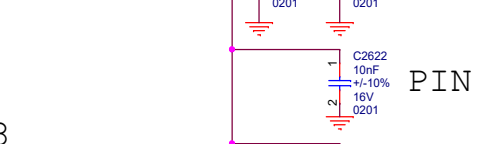
**1.8V\_XO**



**3.3V\_CH1**

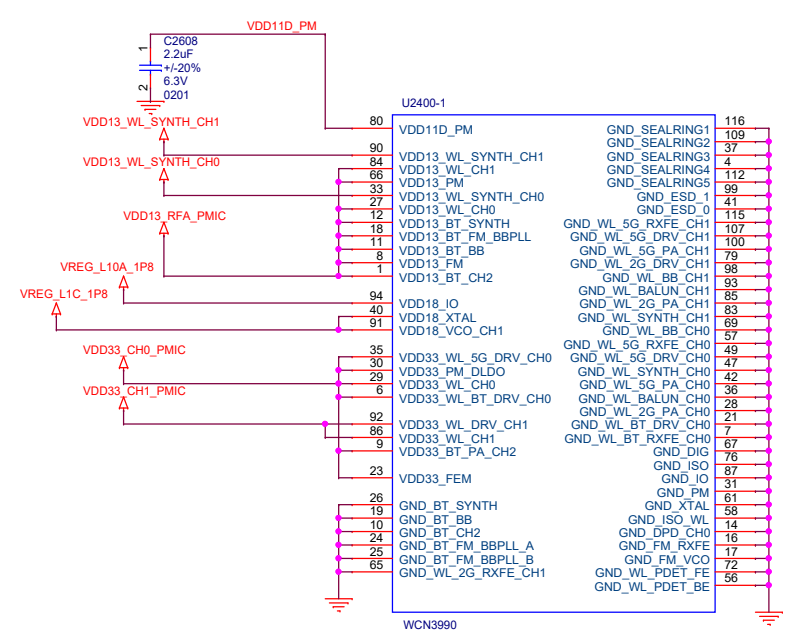


**3.3V\_CH0**



PIN 40

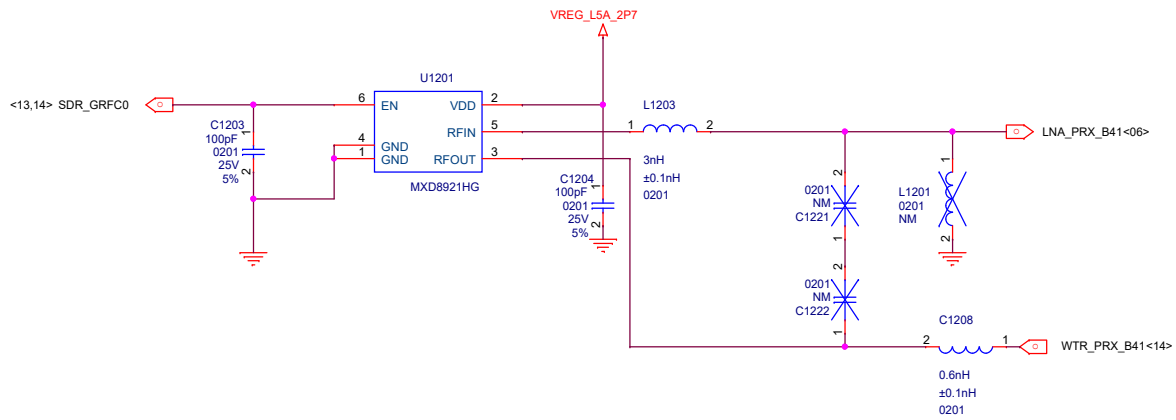
PIN 91



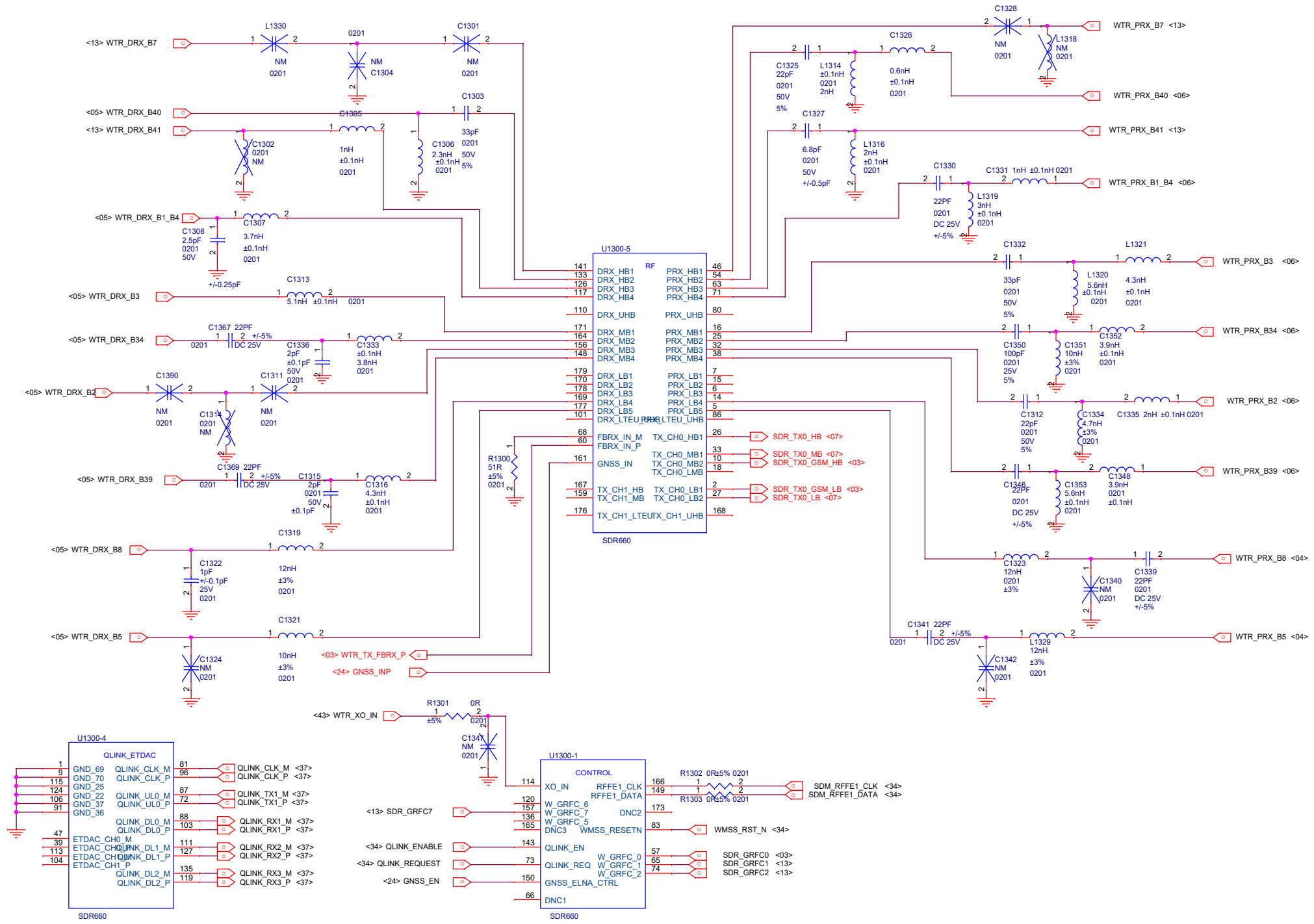
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VDD11D_PM	109	GND_SEALRING2
VDD13_WL_SYNT_CH1	37	GND_SEALRING3
VDD13_WL_CH1	4	GND_SEALRING4
VDD13_PM	112	GND_SEALRING5
VDD13_WL_SYNT_CH0	99	GND_ESD_1
VDD13_WL_CH0	41	GND_ESD_0
VDD13_BT_SYNT	115	GND_WL_5G_RXFE_CH1
VDD13_BT_FM_BBPLL	107	GND_WL_5G_DRV_CH1
VDD13_BT_BB	100	GND_WL_5G_PA_CH1
VDD13_FM	79	GND_WL_2G_DRV_CH1
VDD13_BT_CH2	98	GND_WL_BB_CH1
VDD18_IO	93	GND_WL_BALUN_CH1
VDD18_XTAL	85	GND_WL_2G_PA_CH1
VDD18_VCO_CH1	83	GND_WL_SYNT_CH1
VDD33_CH0_PMIC	69	GND_WL_BB_CH0
VDD33_WL_5G_DRV_CH0	57	GND_WL_5G_RXFE_CH0
VDD33_PM_DLDO	49	GND_WL_5G_DRV_CH0
VDD33_WL_CH0	47	GND_WL_SYNT_CH0
VDD33_WL_BT_DRV_CH0	42	GND_WL_5G_PA_CH0
VDD33_WL_DRV_CH1	36	GND_WL_BALUN_CH0
VDD33_WL_CH1	38	GND_WL_2G_PA_CH0
VDD33_BT_PA_CH2	21	GND_WL_BT_DRV_CH0
VDD33_FEM	7	GND_WL_BT_RXFE_CH0
GND_BT_SYNT	67	GND_DIG
GND_BT_BB	76	GND_ISO
GND_BT_CH2	87	GND_IO
GND_BT_FM_BBPLL_A	31	GND_PM
GND_BT_FM_BBPLL_B	61	GND_XTAL
GND_WL_2G_RXFE_CH1	58	GND_ISO_WL
GND_WL_PDDET_FE	14	GND_DPDP_CH0
GND_WL_PDDET_BE	16	GND_FM_RXFE
	17	GND_FM_VCO
	72	GND_WL_PDDET_FE
	56	GND_WL_PDDET_BE

WCN3990





TP1215	1	TP0.3mm	SDR_GRFC0	<03>
TP1216	1	TP0.3mm	SDR_GRFC1	<13>
TP1217	1	TP0.3mm	SDR_GRFC2	<13>



D

D

C

C

B

B

A

A

5

4

3

2

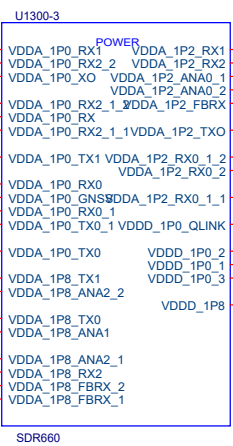
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VREG\_L2A\_1P0



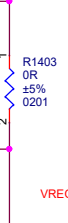
CAD NOTE: Dotted box represent SDR660 power supply star routing



VREG\_L1A\_1P2



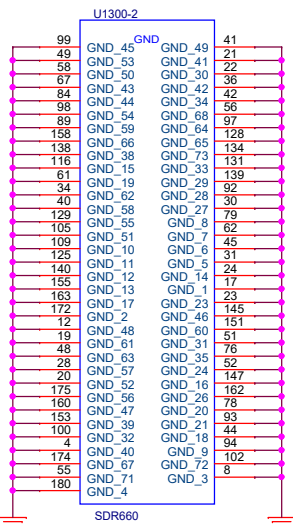
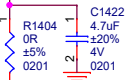
VREG\_L3A\_1P0



VREG\_L14A\_1P8



VREG\_L10A\_1P8



D

C

B

A

D

C

B

A

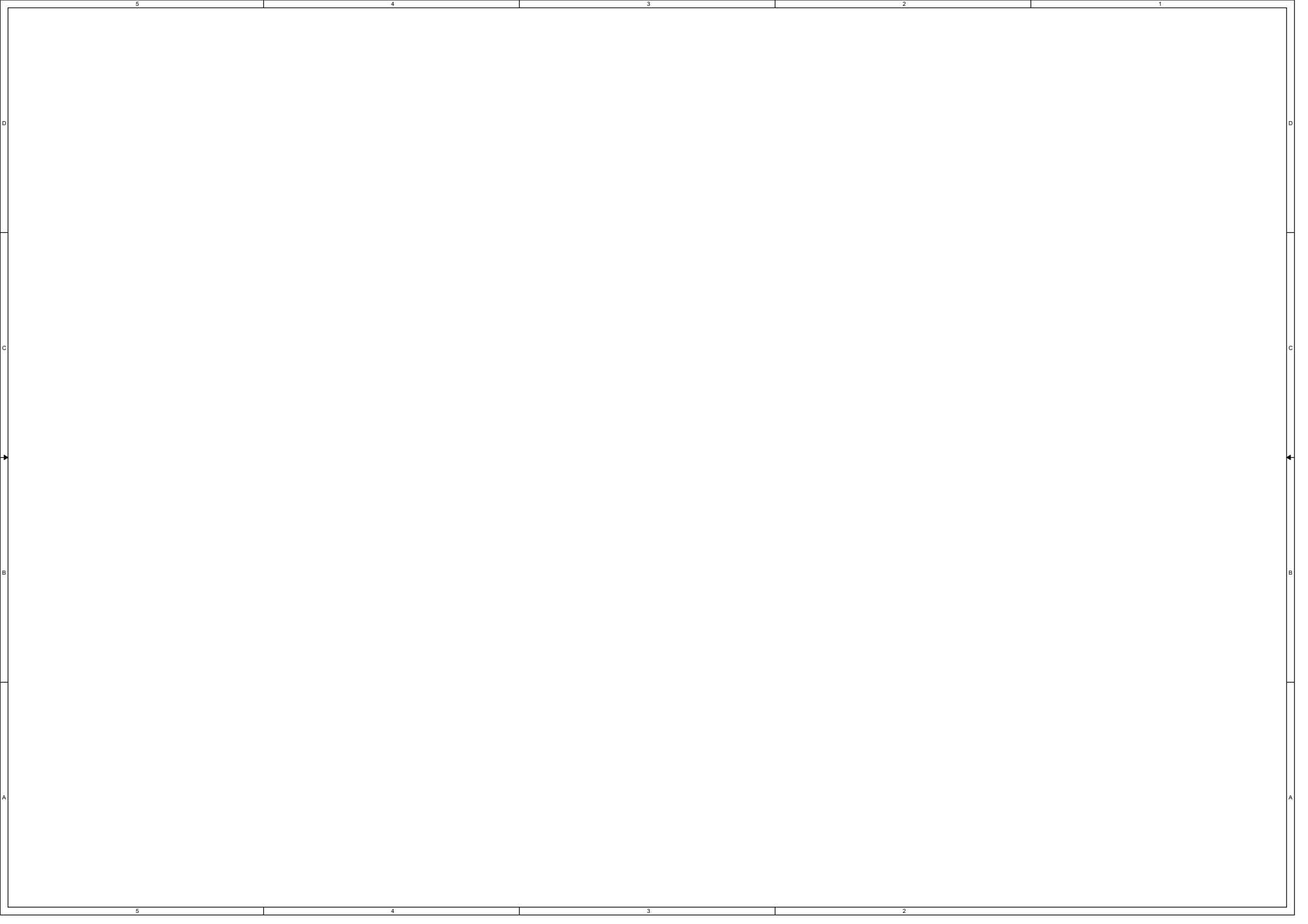
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4

3

2

1







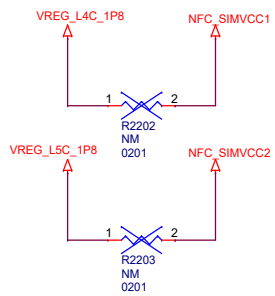
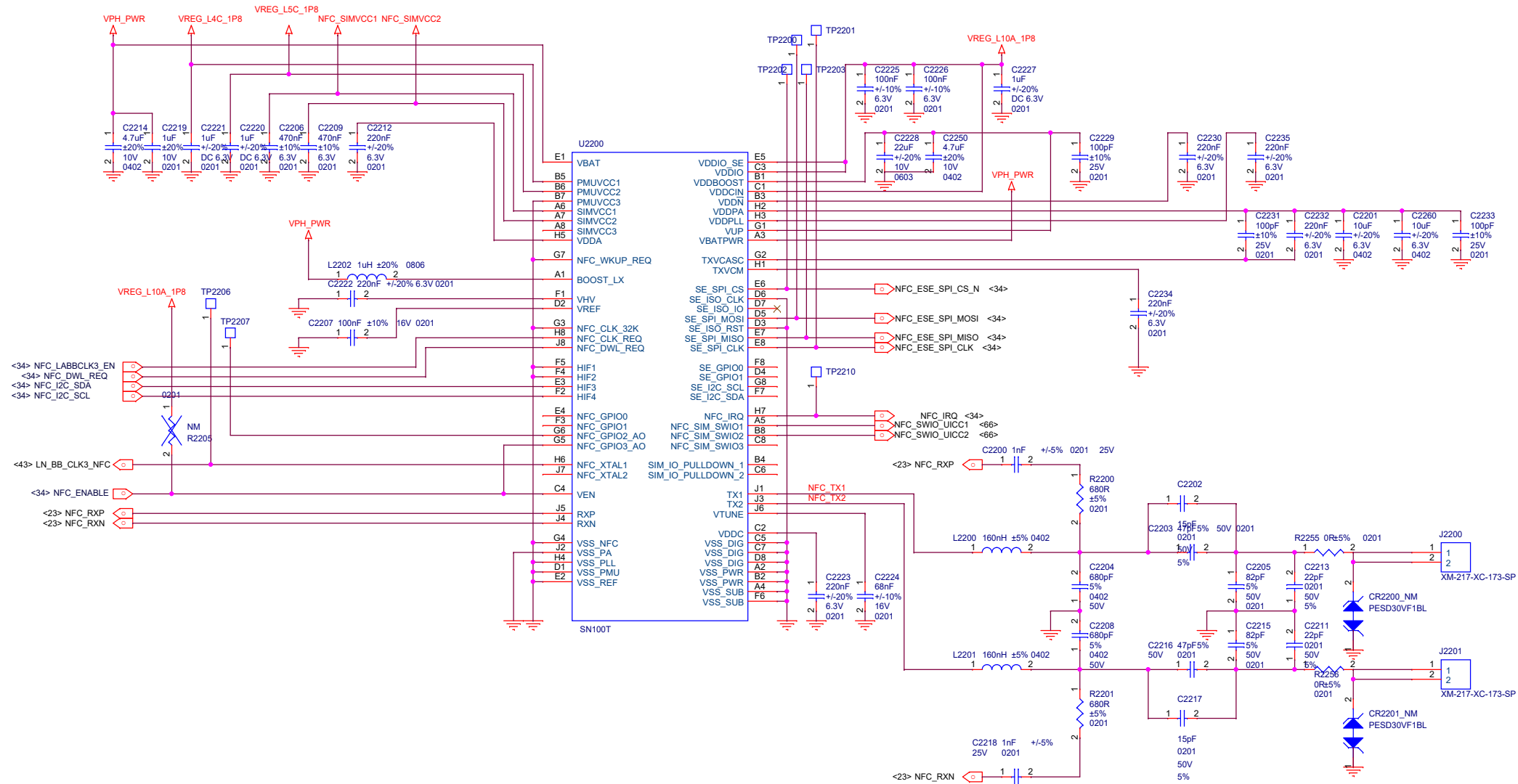


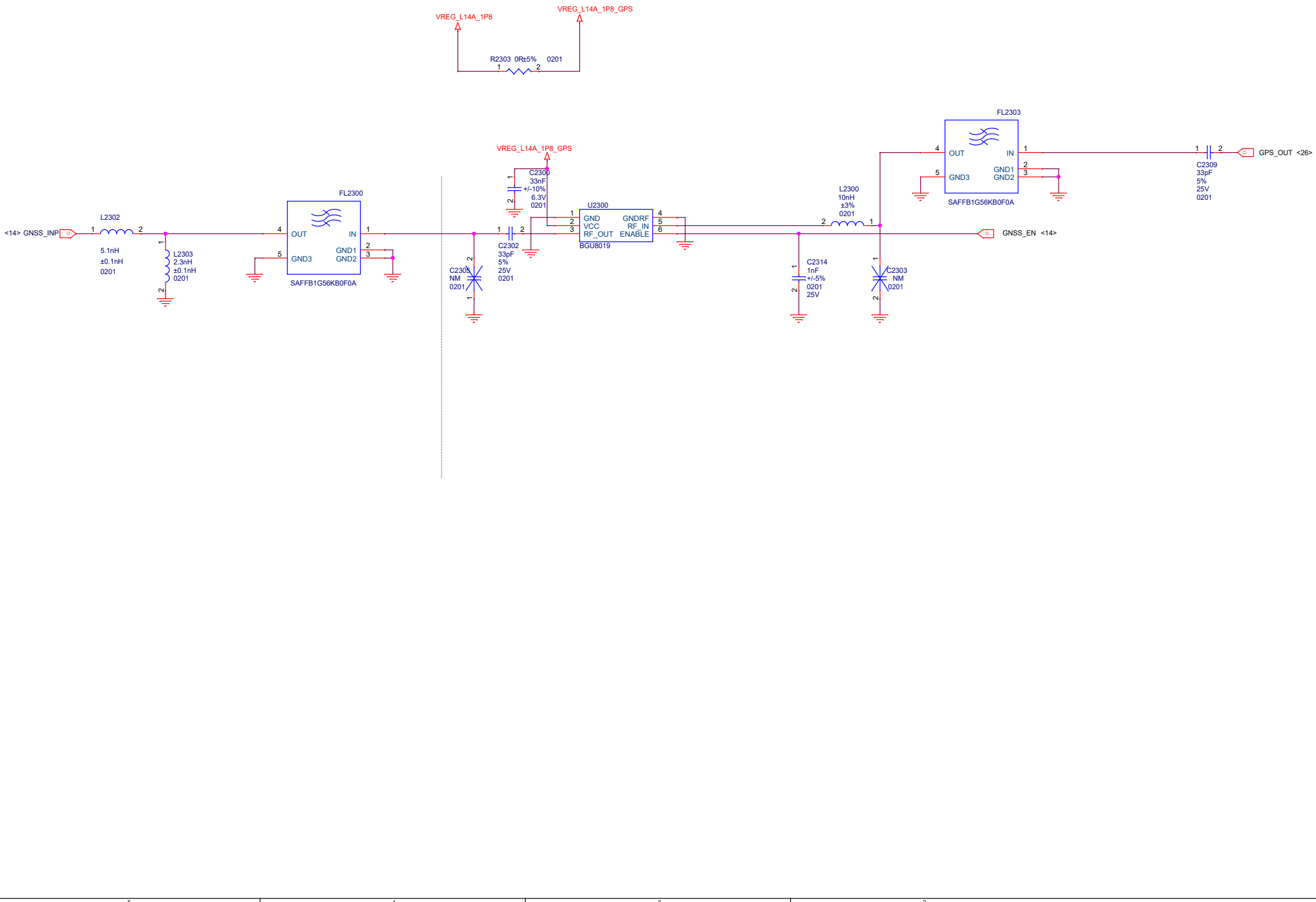


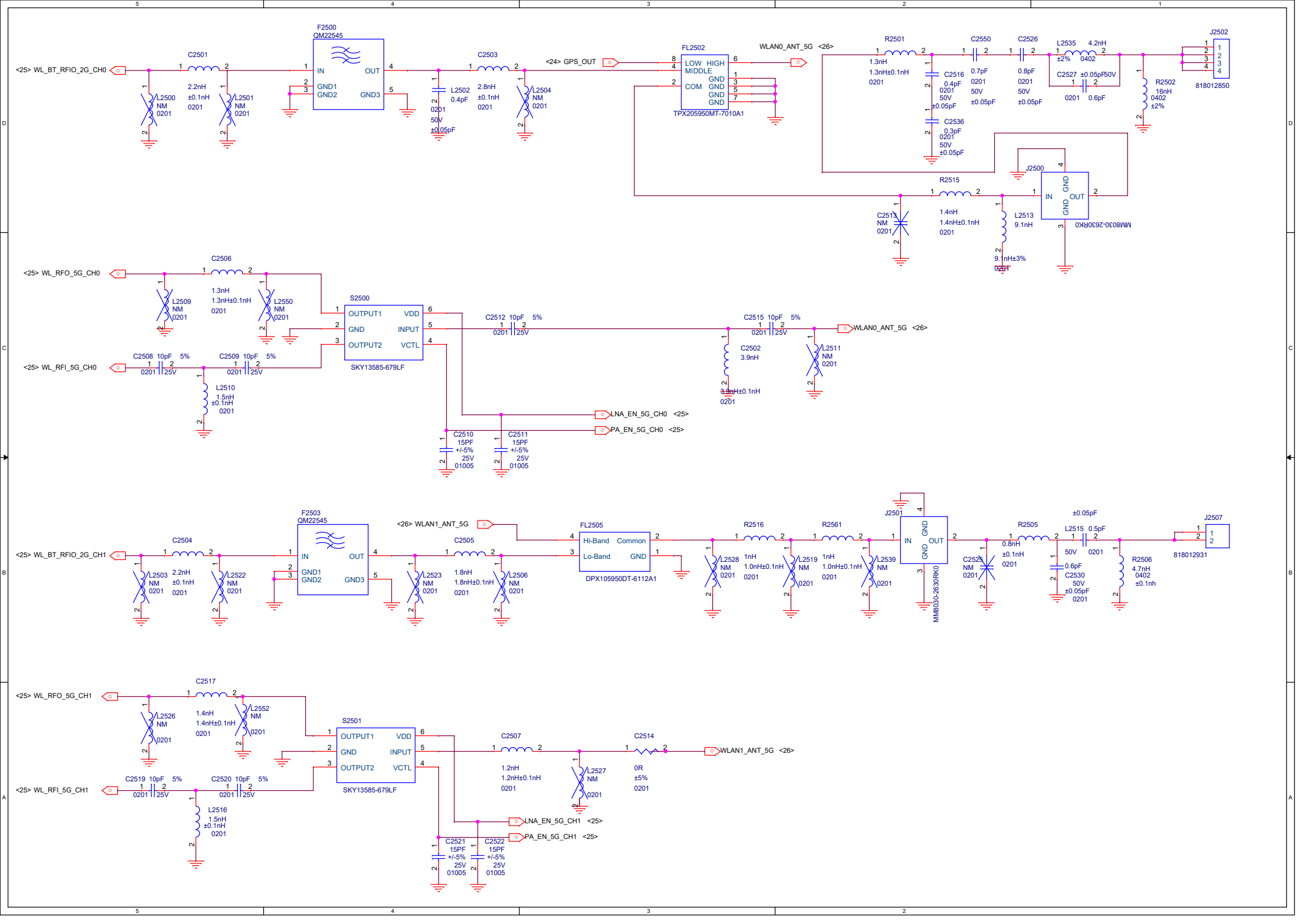












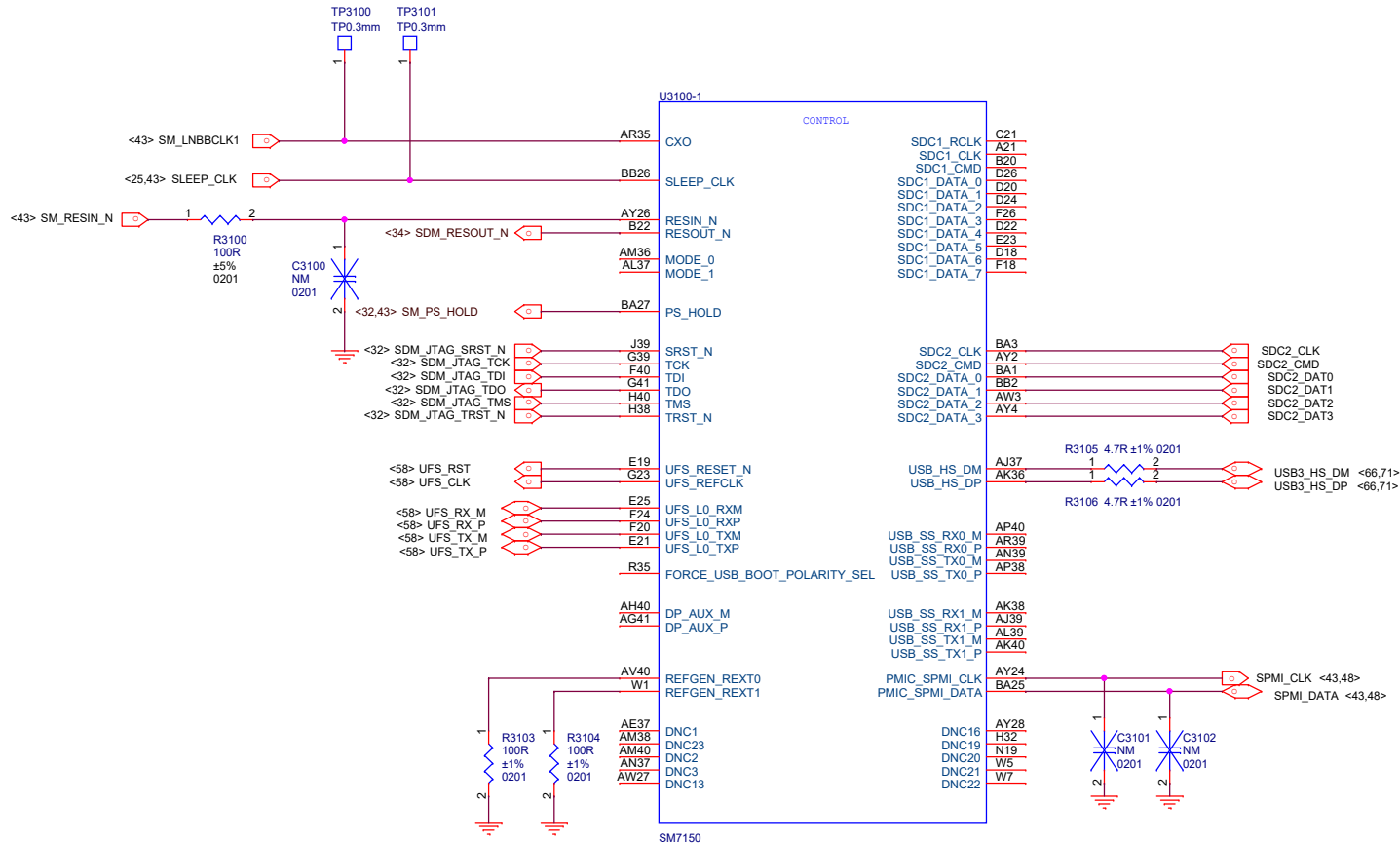






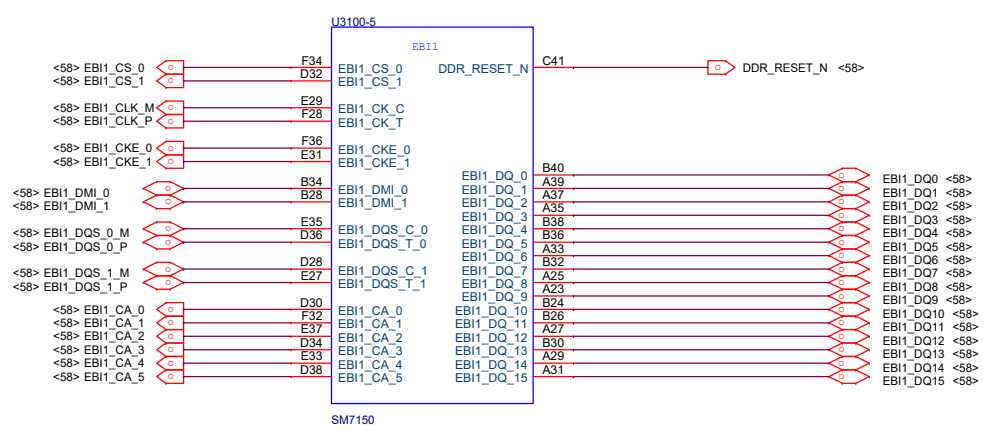
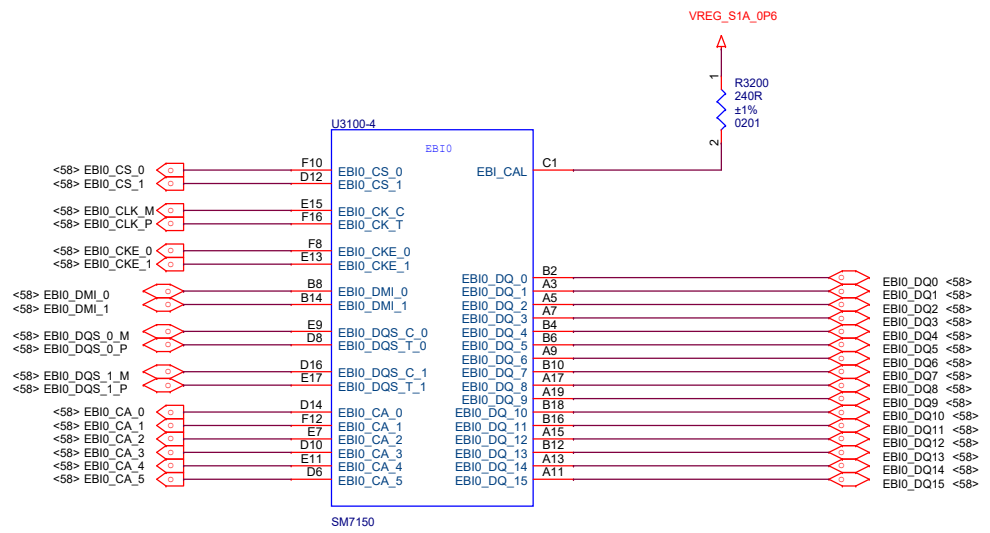


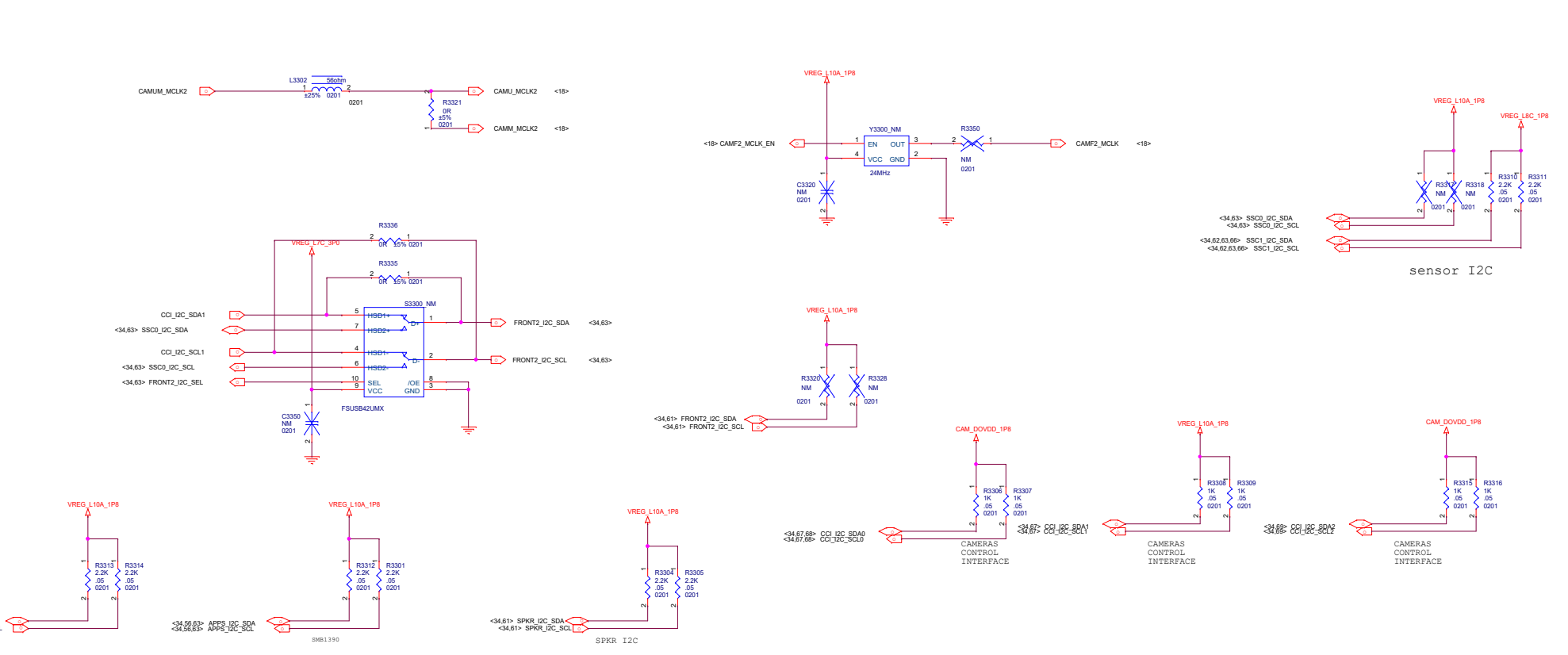
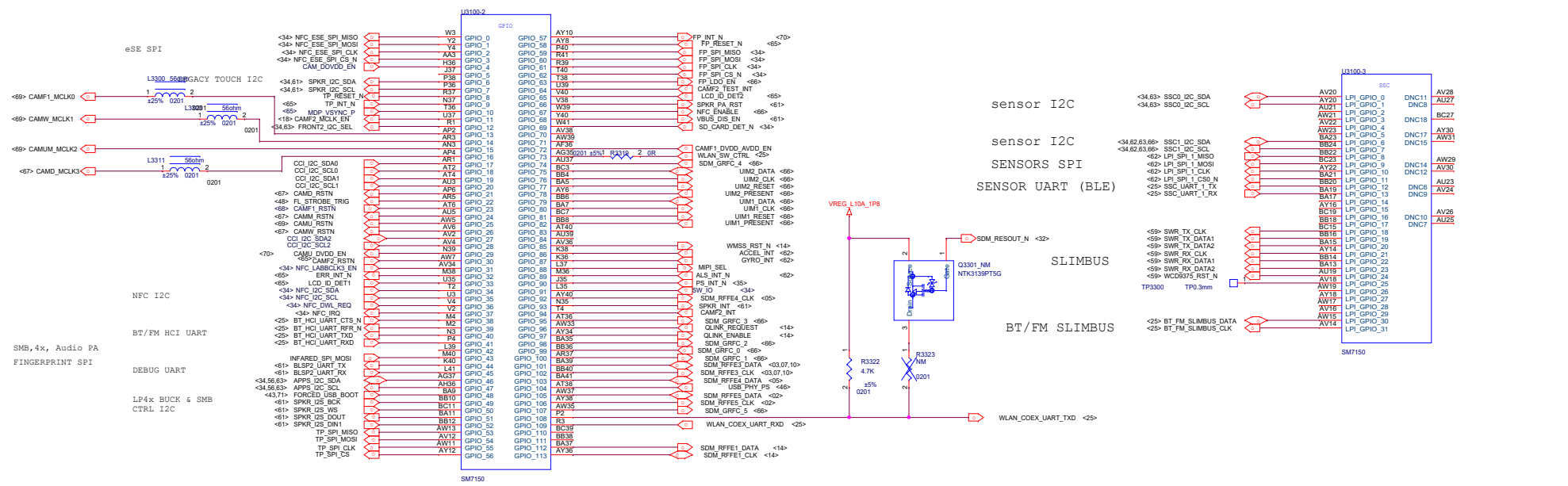
MODE	Operation
00	NATIVE
01	TIC
10	ATEST
11	TEST



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FRONT1 CAMERA  
20M

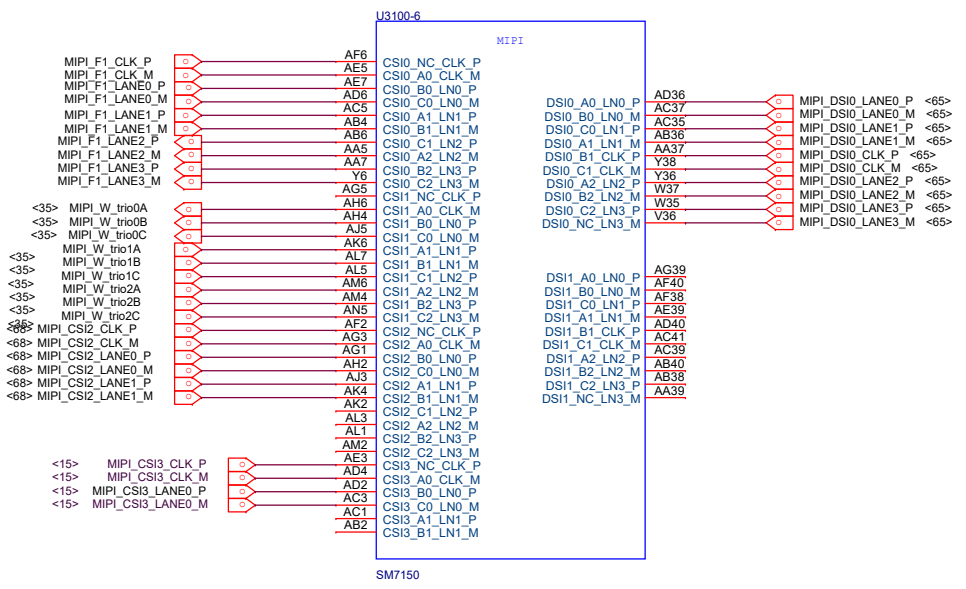
WIDE CAMERA  
IMX686 64M

ULTRA CAMERA  
8M

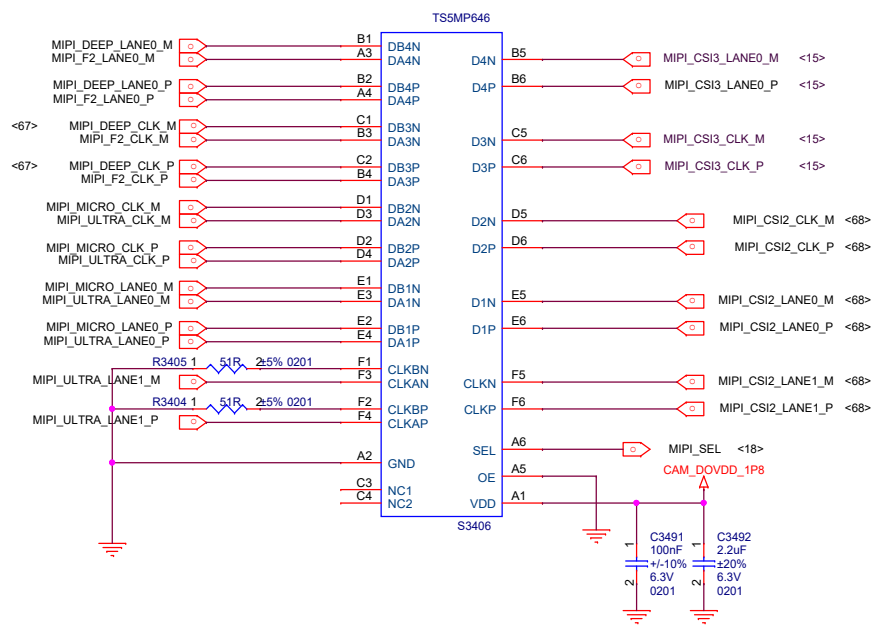
MICRO CAMERA  
2M

DEEP CAMERA  
2M

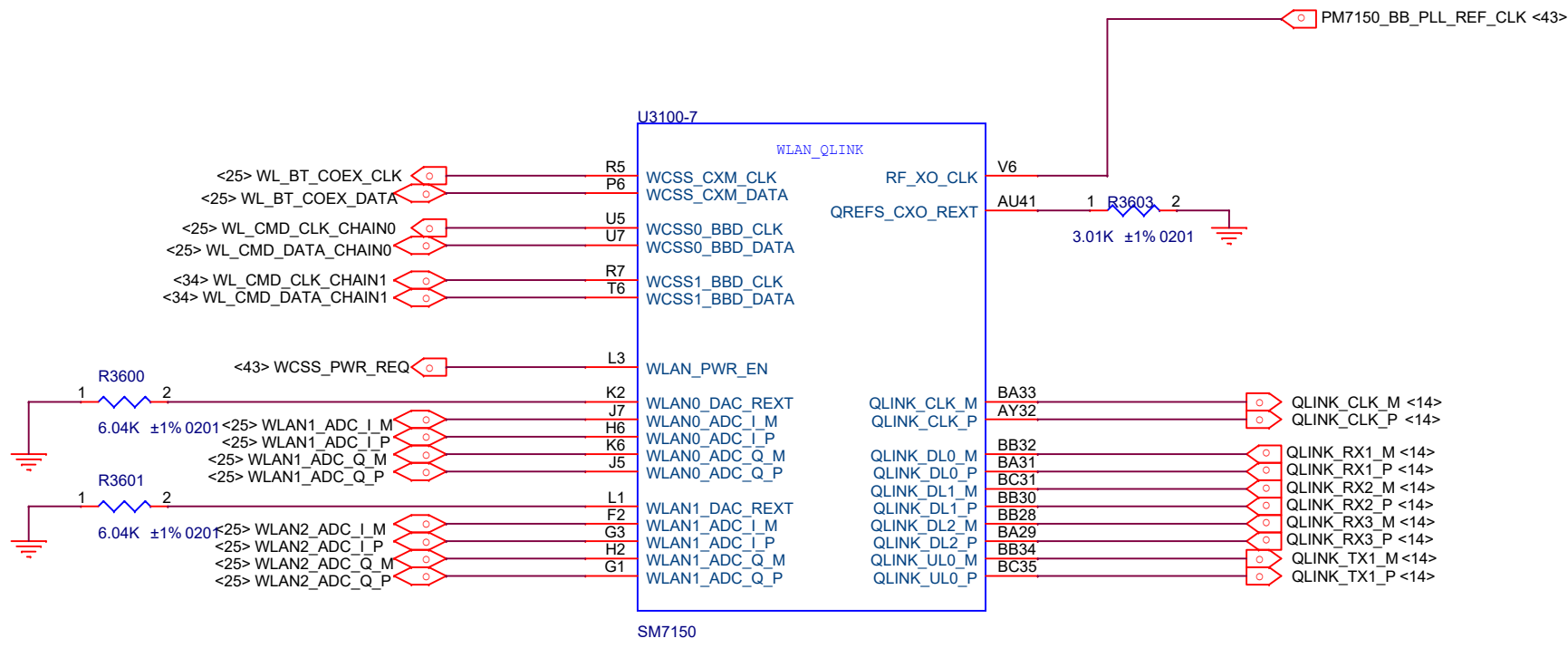
FRONT2 CAMERA  
2M

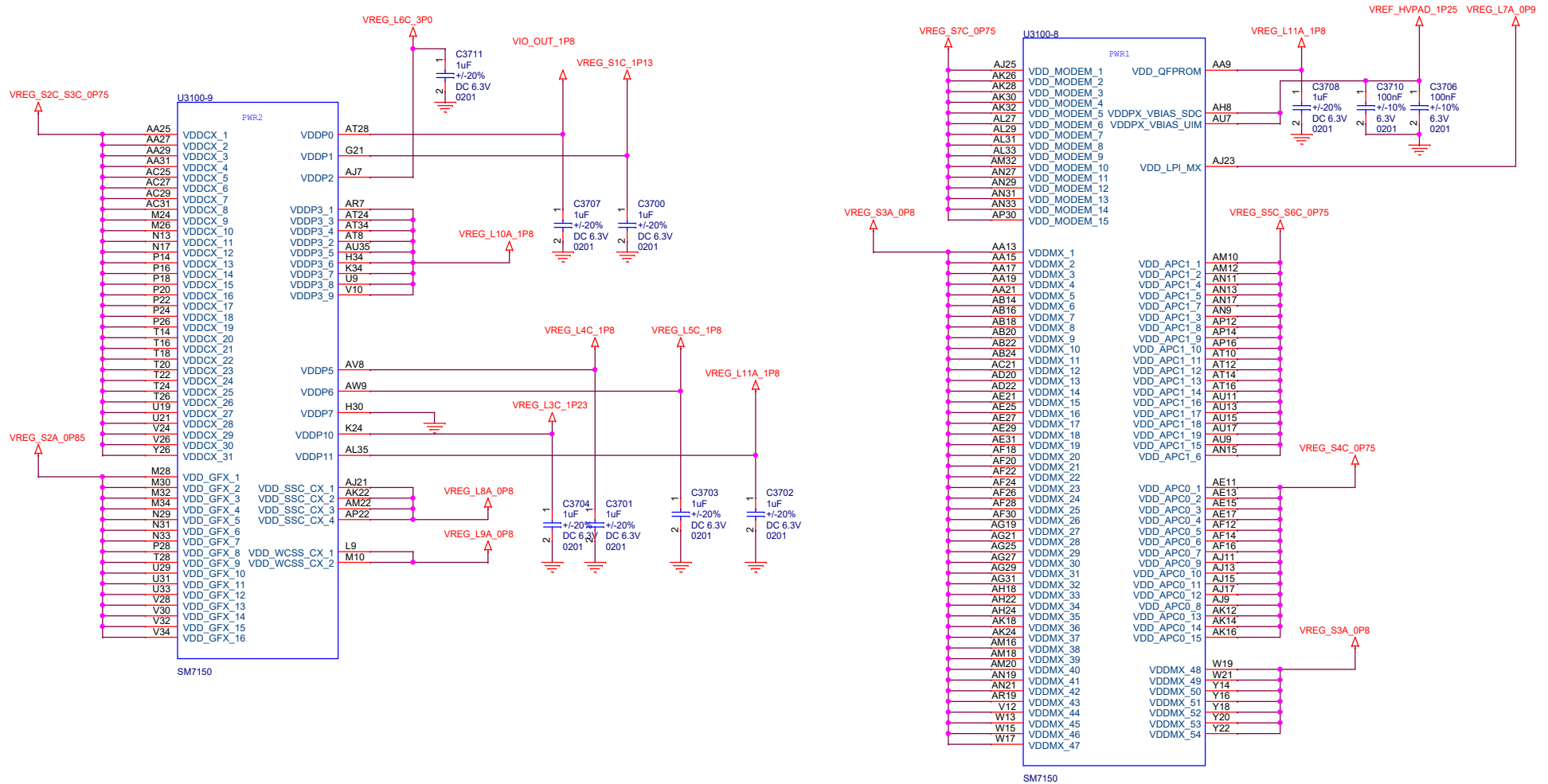


MIPI SWITCH



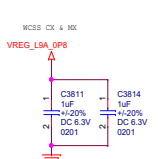
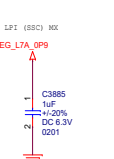
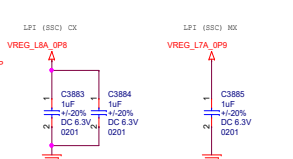
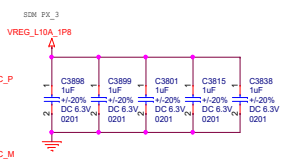
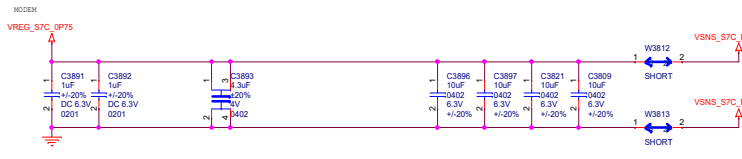
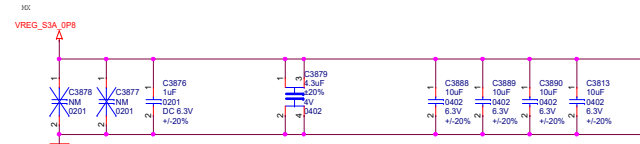
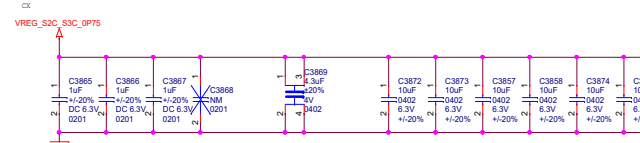
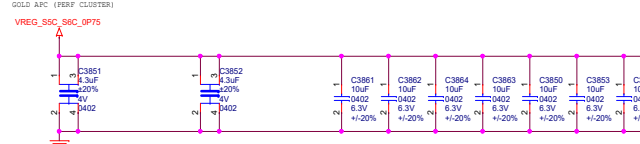
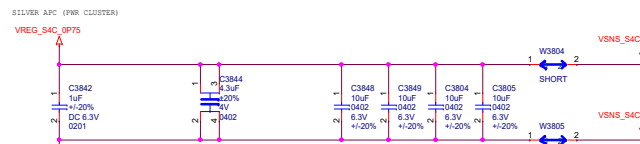
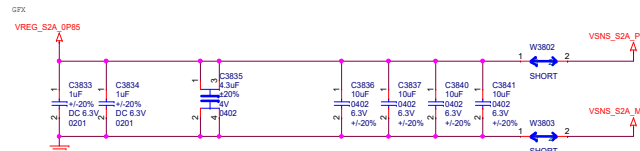
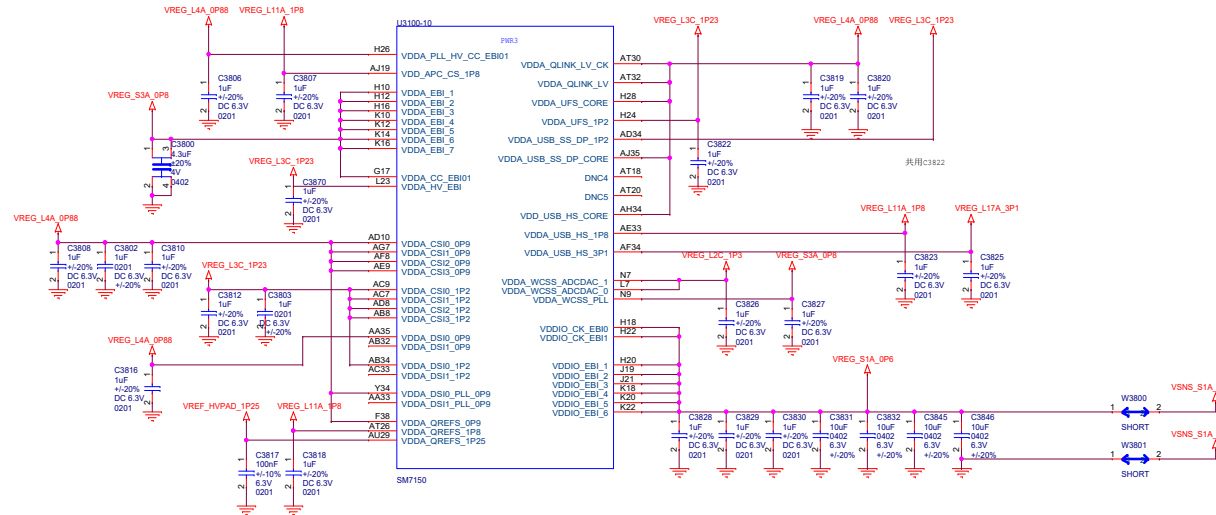






Pin	IC Pin	IC Pin	IC Pin
AA25	VDDCX_1	VDDP0	AT28
AA27	VDDCX_2	VDDP1	G21
AA29	VDDCX_3	VDDP2	AJ7
AA31	VDDCX_4		
AC25	VDDCX_5		
AC27	VDDCX_6		
AC29	VDDCX_7		
AC31	VDDCX_8	VDDP3_1	AR7
M24	VDDCX_9	VDDP3_3	AT24
N13	VDDCX_10	VDDP3_4	AT34
N17	VDDCX_11	VDDP3_2	AT8
P14	VDDCX_12	VDDP3_5	AU35
P16	VDDCX_13	VDDP3_6	H34
P18	VDDCX_14	VDDP3_7	K34
P20	VDDCX_15	VDDP3_8	U9
P22	VDDCX_16	VDDP3_9	V10
P24	VDDCX_17		
P26	VDDCX_18		
T14	VDDCX_19		
T16	VDDCX_20		
T18	VDDCX_21		
T20	VDDCX_22		
T22	VDDCX_23	VDDP5	AV8
T24	VDDCX_24	VDDP6	AW9
T26	VDDCX_25	VDDP7	H30
U19	VDDCX_26	VDDP10	K24
U21	VDDCX_27	VDDP11	AL35
U24	VDDCX_28		
V26	VDDCX_29		
Y26	VDDCX_30		
	VDDCX_31		
M28	VDD_GFX_1	VDD_SSC_CX_1	AJ21
M30	VDD_GFX_2	VDD_SSC_CX_2	AK22
M32	VDD_GFX_3	VDD_SSC_CX_3	AM22
M34	VDD_GFX_4	VDD_SSC_CX_4	AP22
N29	VDD_GFX_5		
N31	VDD_GFX_6		
N33	VDD_GFX_7		
P28	VDD_GFX_8	VDD_WCSS_CX_1	L9
T28	VDD_GFX_9	VDD_WCSS_CX_2	M10
U29	VDD_GFX_10		
U31	VDD_GFX_11		
U33	VDD_GFX_12		
V28	VDD_GFX_13		
V30	VDD_GFX_14		
V32	VDD_GFX_15		
V34	VDD_GFX_16		

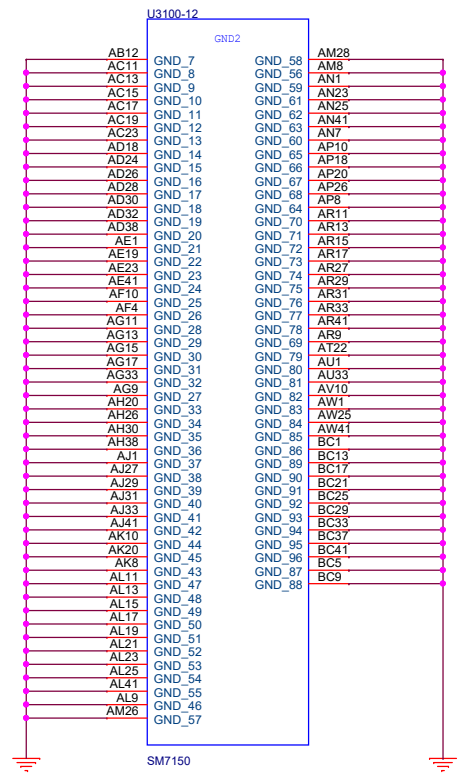
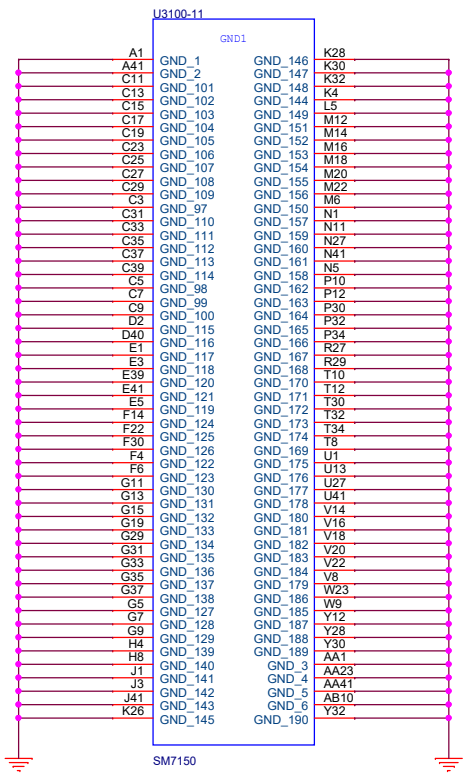
Pin	IC Pin	IC Pin	IC Pin
AJ25	VDD_MODEM_1	VDD_QFPROM	AA9
AK26	VDD_MODEM_2		
AK28	VDD_MODEM_3		
AK30	VDD_MODEM_4		
AK32	VDD_MODEM_5	VDDPX_VBIAS_SDC	AH8
AL27	VDD_MODEM_6	VDDPX_VBIAS_UIM	AU7
AL29	VDD_MODEM_7		
AL31	VDD_MODEM_8		
AL33	VDD_MODEM_9		
AM32	VDD_MODEM_10	VDD_LPI_MX	AJ23
AN27	VDD_MODEM_11		
AN29	VDD_MODEM_12		
AN31	VDD_MODEM_13		
AN33	VDD_MODEM_14		
AP30	VDD_MODEM_15		
AA13	VDDMX_1		
AA15	VDDMX_2		
AA17	VDDMX_3		
AA19	VDDMX_4		
AA21	VDDMX_5		
AB14	VDDMX_6		
AB16	VDDMX_7		
AB18	VDDMX_8		
AB20	VDDMX_9		
AB22	VDDMX_10		
AB24	VDDMX_11		
AC21	VDDMX_12		
AD20	VDDMX_13		
AD22	VDDMX_14		
AE21	VDDMX_15		
AE25	VDDMX_16		
AE27	VDDMX_17		
AE29	VDDMX_18		
AE31	VDDMX_19		
AF18	VDDMX_20		
AF20	VDDMX_21		
AF22	VDDMX_22		
AF24	VDDMX_23		
AF26	VDDMX_24		
AF28	VDDMX_25		
AF30	VDDMX_26		
AG19	VDDMX_27		
AG21	VDDMX_28		
AG25	VDDMX_29		
AG27	VDDMX_30		
AG29	VDDMX_31		
AG31	VDDMX_32		
AH18	VDDMX_33		
AH22	VDDMX_34		
AH24	VDDMX_35		
AK18	VDDMX_36		
AK24	VDDMX_37		
AM16	VDDMX_38		
AM18	VDDMX_39		
AM20	VDDMX_40		
AN19	VDDMX_41		
AN21	VDDMX_42		
AR19	VDDMX_43		
V12	VDDMX_44		
W13	VDDMX_45		
W15	VDDMX_46		
W17	VDDMX_47		
AA10	VDD_APC1_1		
AA12	VDD_APC1_2		
AN11	VDD_APC1_3		
AN13	VDD_APC1_4		
AN17	VDD_APC1_5		
AN9	VDD_APC1_7		
AP12	VDD_APC1_8		
AP14	VDD_APC1_9		
AP16	VDD_APC1_10		
AT10	VDD_APC1_11		
AT12	VDD_APC1_12		
AT14	VDD_APC1_13		
AT16	VDD_APC1_14		
AU11	VDD_APC1_16		
AU13	VDD_APC1_17		
AU15	VDD_APC1_18		
AU17	VDD_APC1_19		
AU9	VDD_APC1_15		
AN15	VDD_APC1_6		
AE11	VDD_APC0_1		
AE13	VDD_APC0_2		
AE15	VDD_APC0_3		
AE17	VDD_APC0_4		
AF12	VDD_APC0_5		
AF14	VDD_APC0_6		
AF16	VDD_APC0_7		
AJ11	VDD_APC0_8		
AJ13	VDD_APC0_9		
AJ15	VDD_APC0_10		
AJ17	VDD_APC0_11		
AJ9	VDD_APC0_12		
AK12	VDD_APC0_13		
AK14	VDD_APC0_14		
AK16	VDD_APC0_15		
W19	VDDMX_48		
W21	VDDMX_49		
Y14	VDDMX_50		
Y16	VDDMX_51		
Y18	VDDMX_52		
Y20	VDDMX_53		
Y22	VDDMX_54		

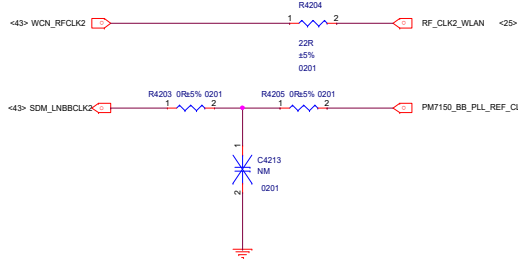
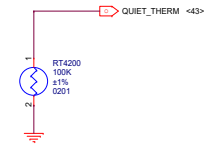
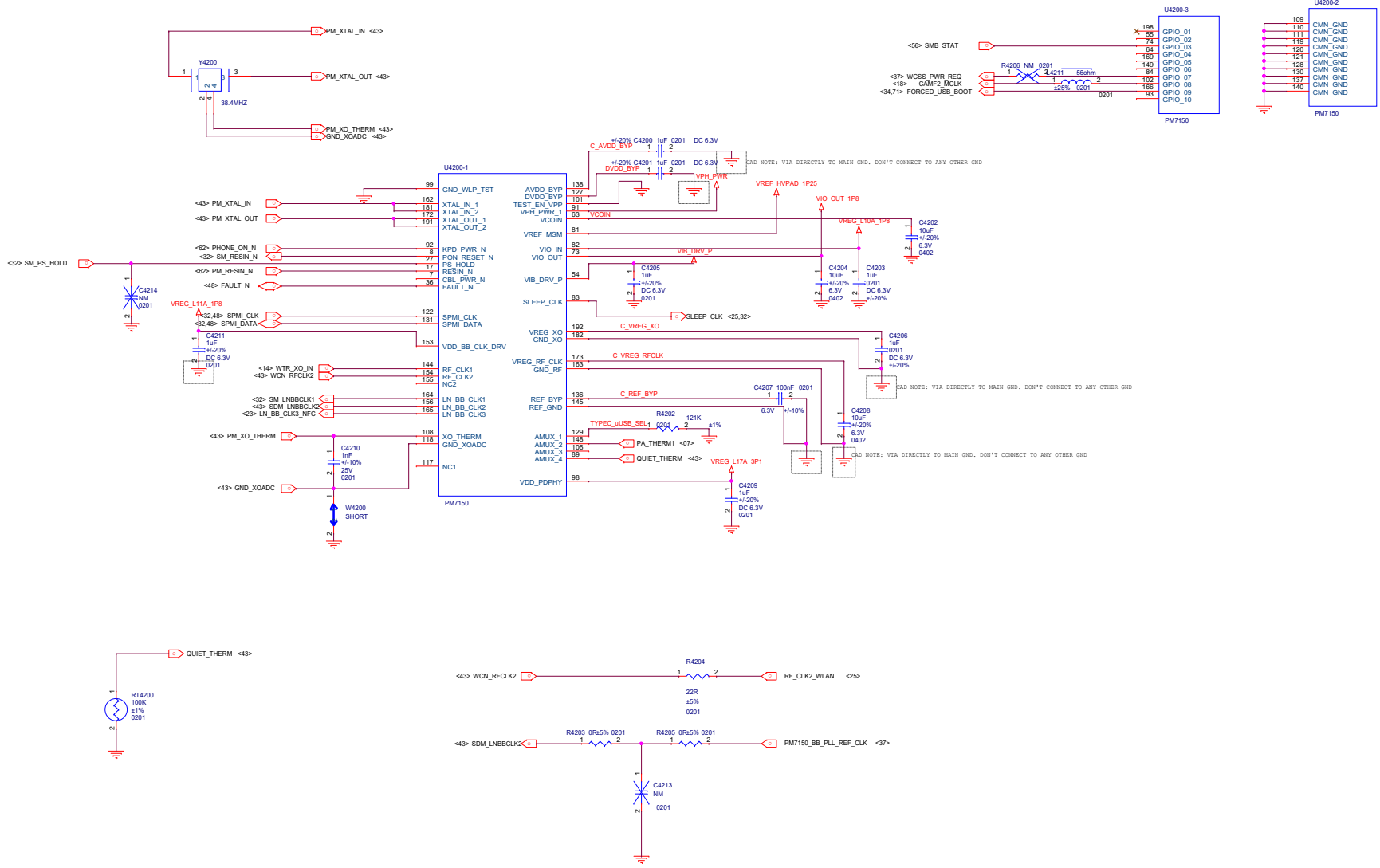


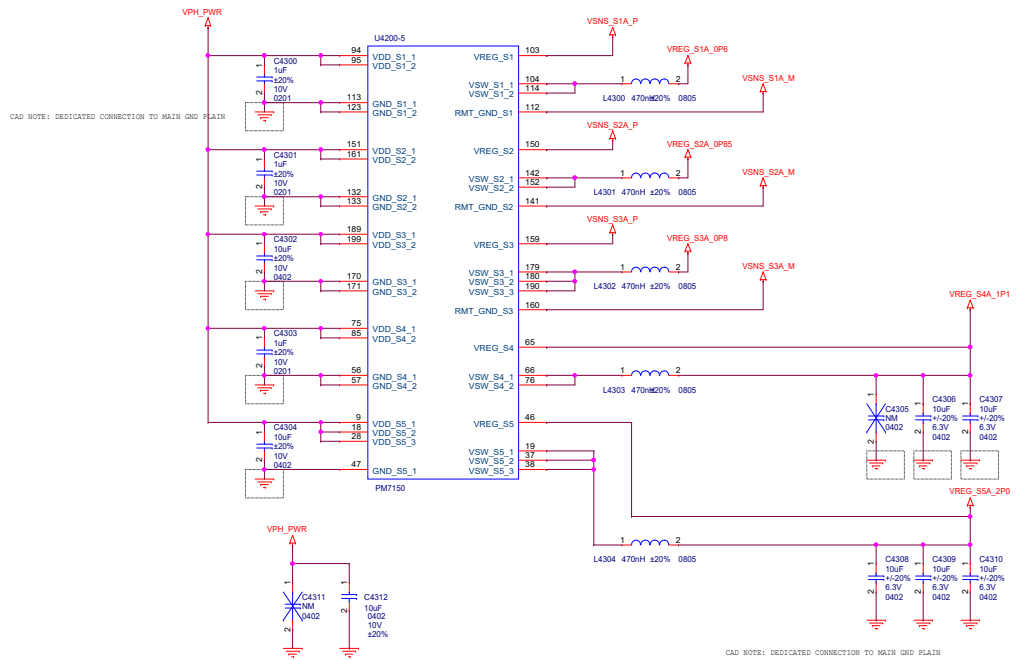


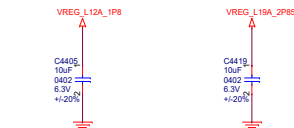
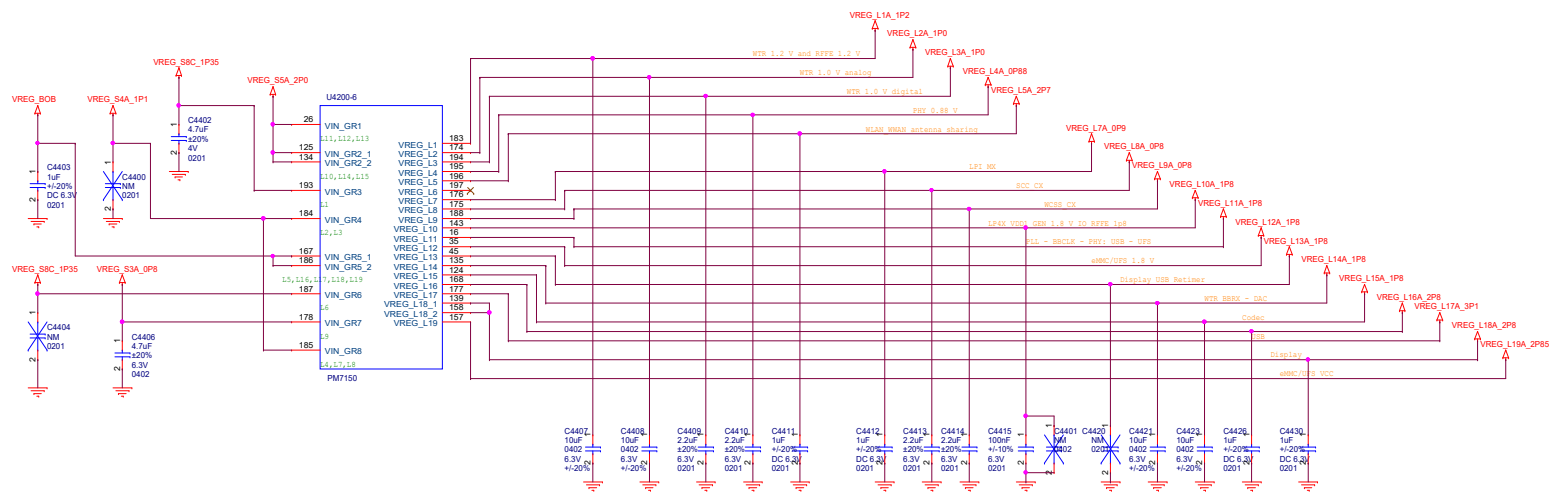




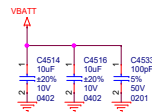
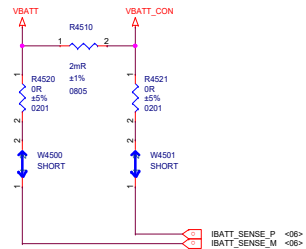
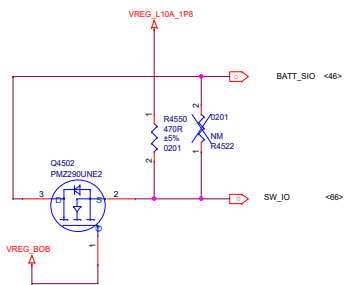
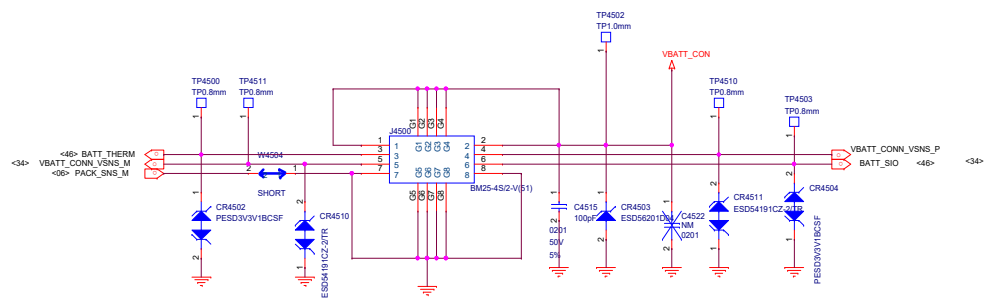
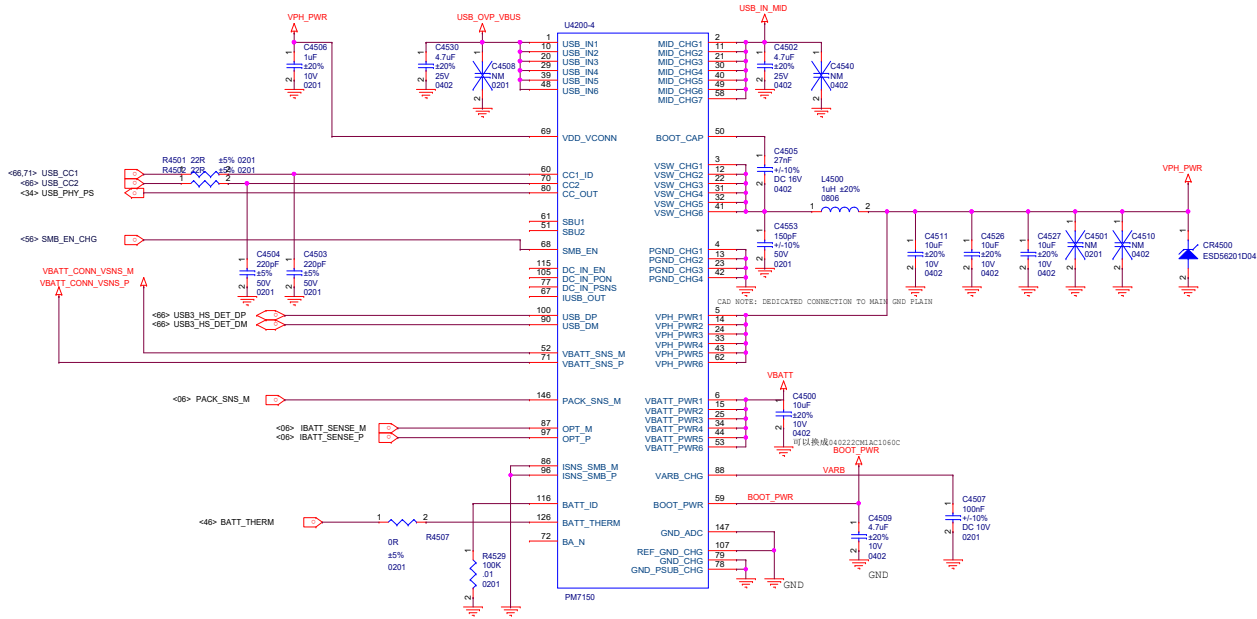








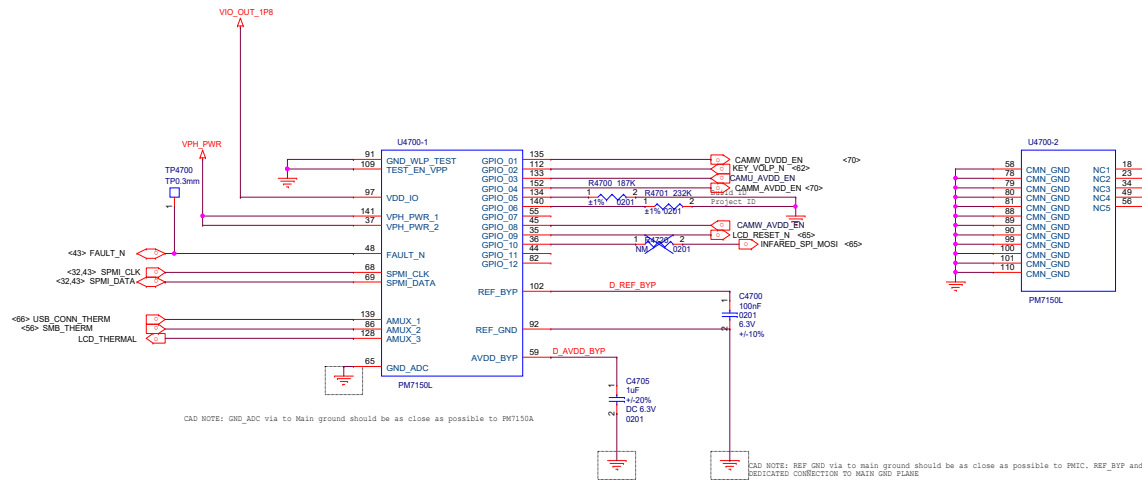
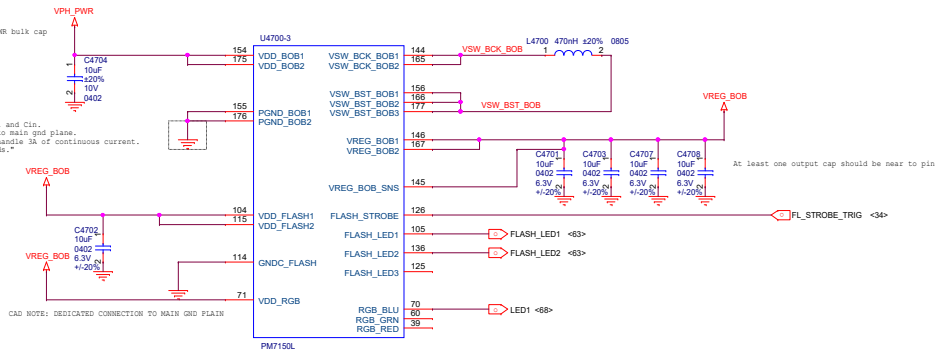
VREG\_L11A\_1P8预留电容删除  
 高度限制, 10uF拆成2个4.7uF  
 PSEUDO CAPLESS LDOs  
 For CAPLESS LDOs: If decaps on the load side do not  
 add up to LDO spec, then install the cap close to the PMIC





CAD Note: Place C4704 right next to the PMIC. This also acts as VPH\_PWR bulk cap

CAD NOTE: Layout Note:PCMD\_BOB  
 \*Dedicated trace from pin to C0001 and Cln.  
 \*Dedicated vias from cap directly to main gnd plane.  
 Trace and vias should be able to handle 3A of continuous current.  
 Do NOT connect to any other grounds.\*



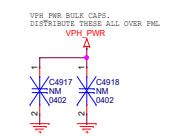
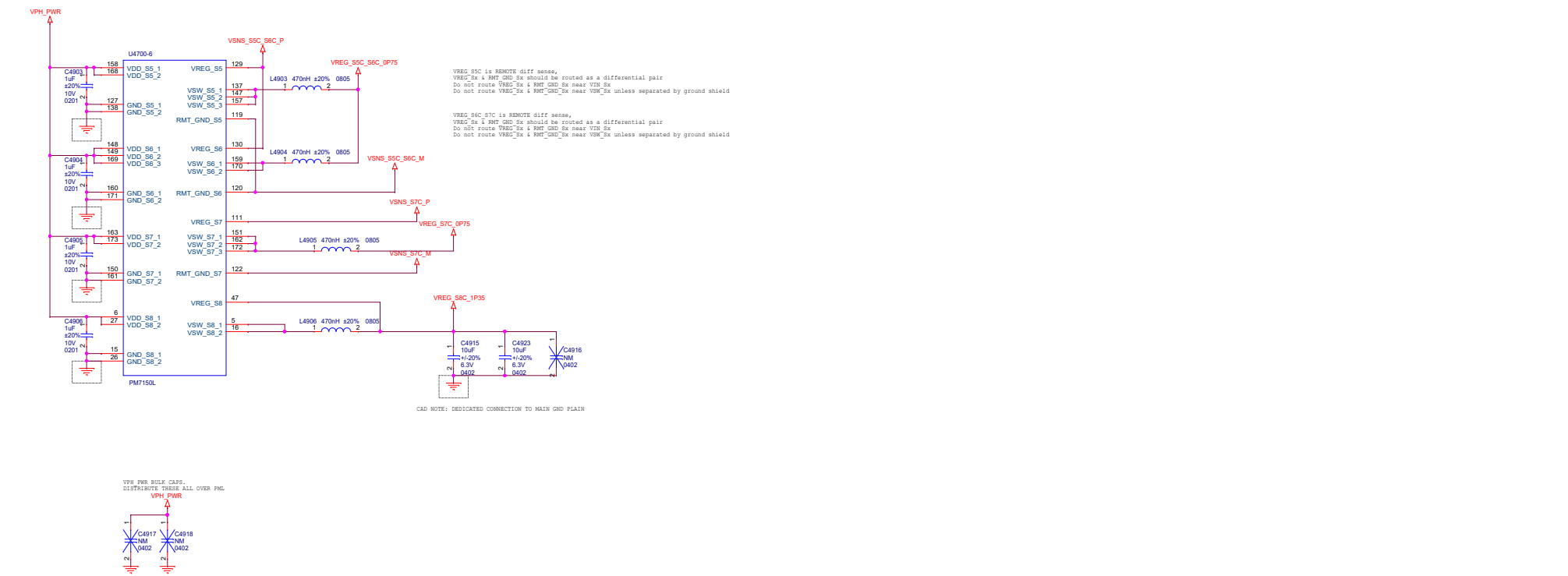
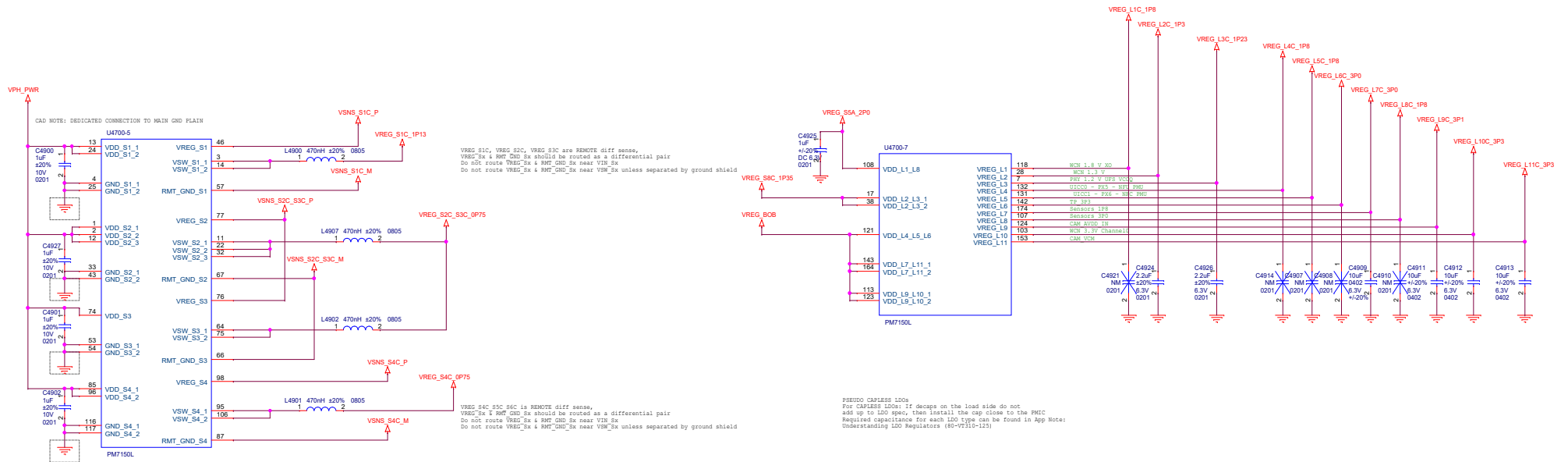
CAD NOTE: GND\_ADC via to Main ground should be as close as possible to PM7150A

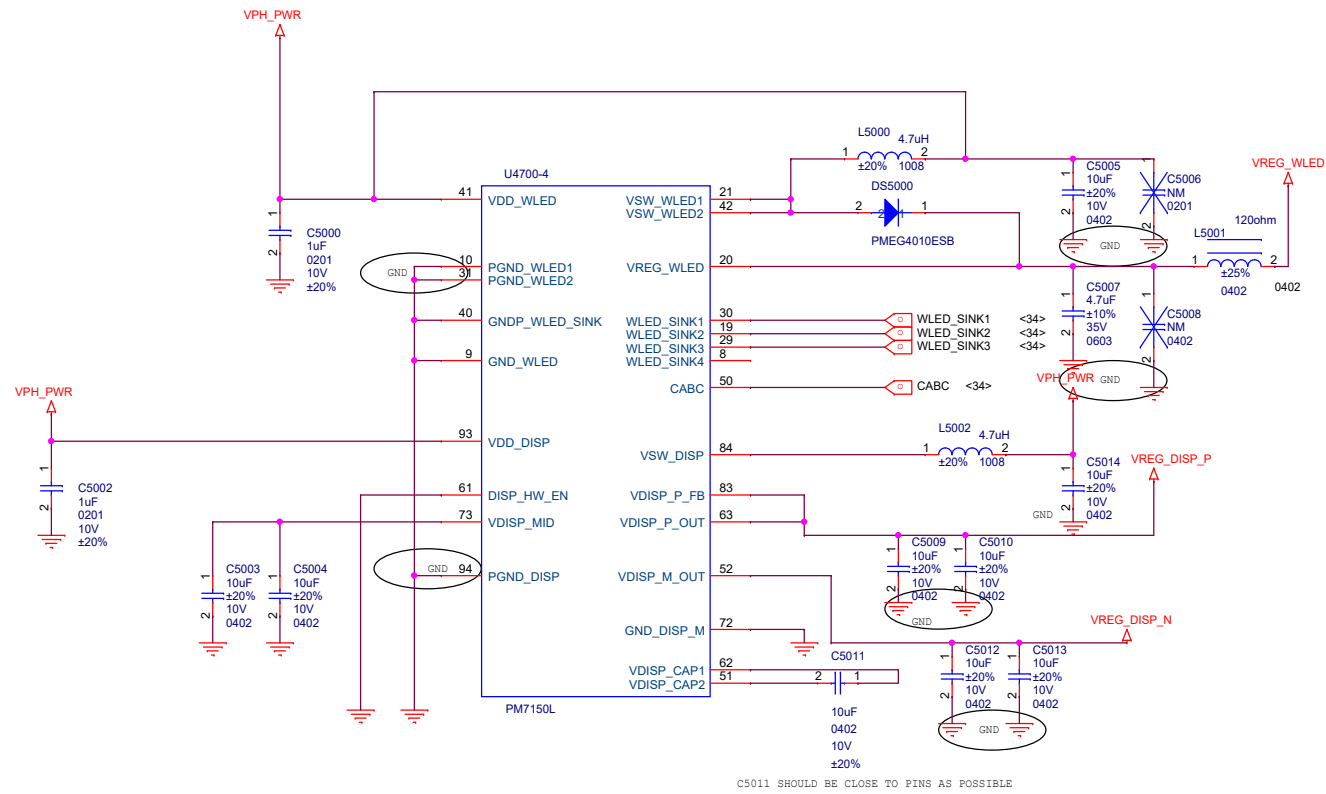
CAD NOTE: REF\_GND via to main ground should be as close as possible to PMIC. REF\_BYP and REF\_GND should be routed away from noisy traces. DEDICATED CONNECTION TO MAIN GND PLANE

CAD NOTE: AVDD\_BYP should be routed away from noisy traces . DEDICATED CONNECTION TO MAIN GND PLANE









C5011 SHOULD BE CLOSE TO PINS AS POSSIBLE

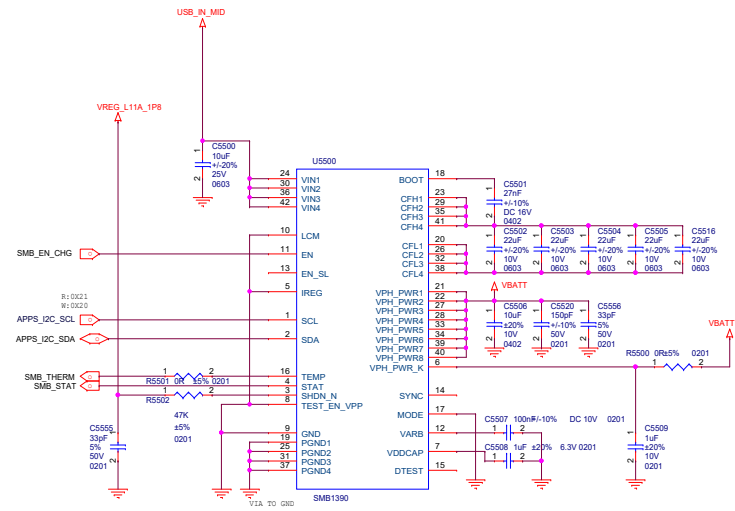
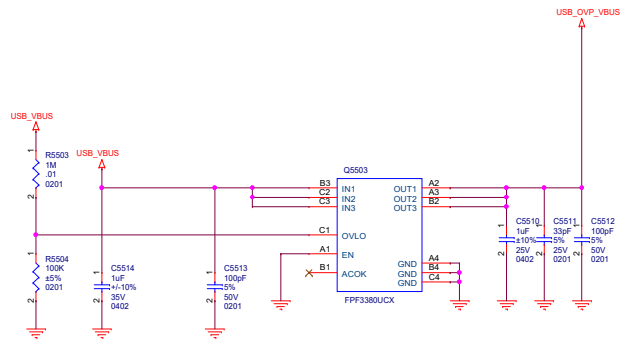




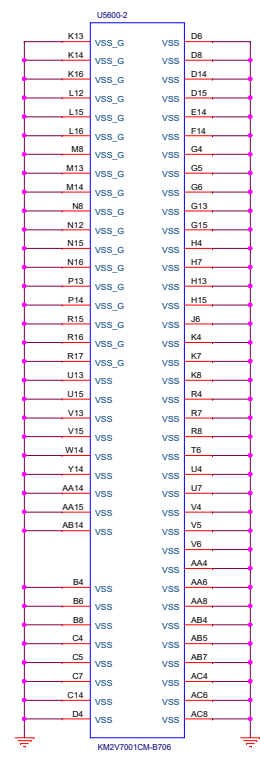
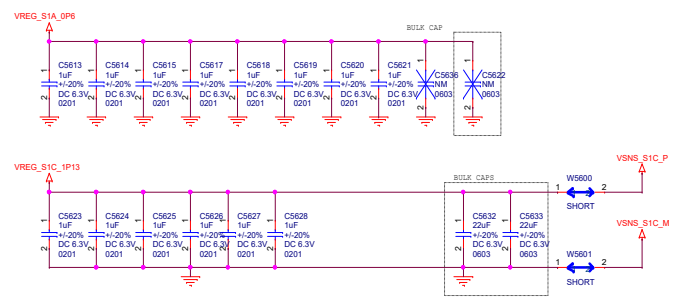
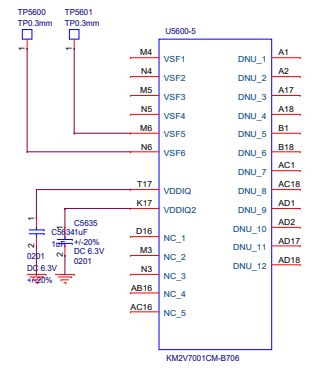
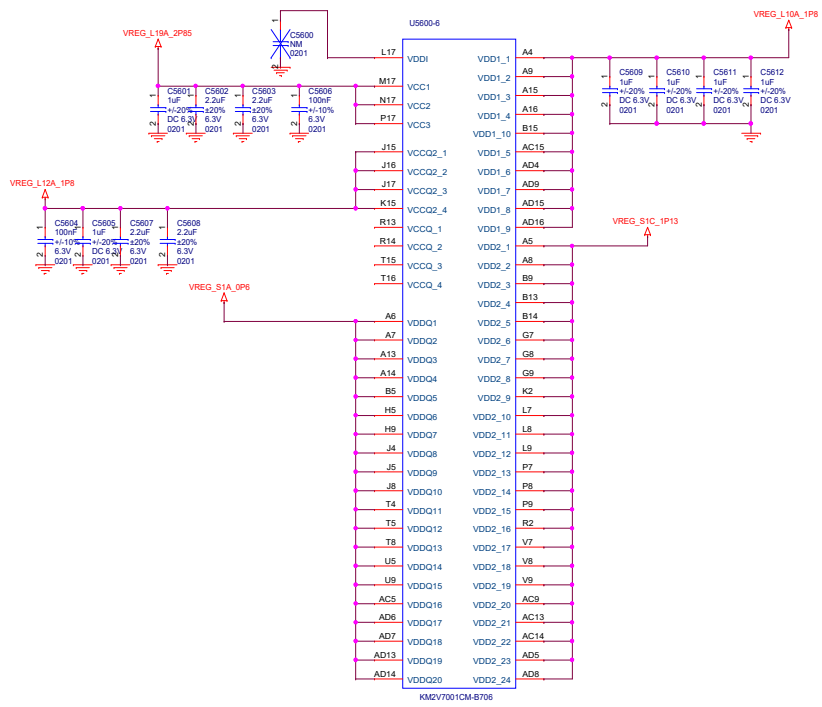


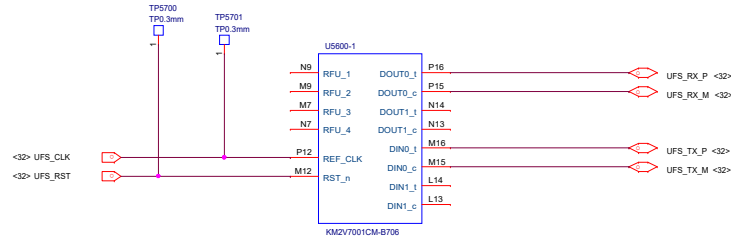


# SMB1390

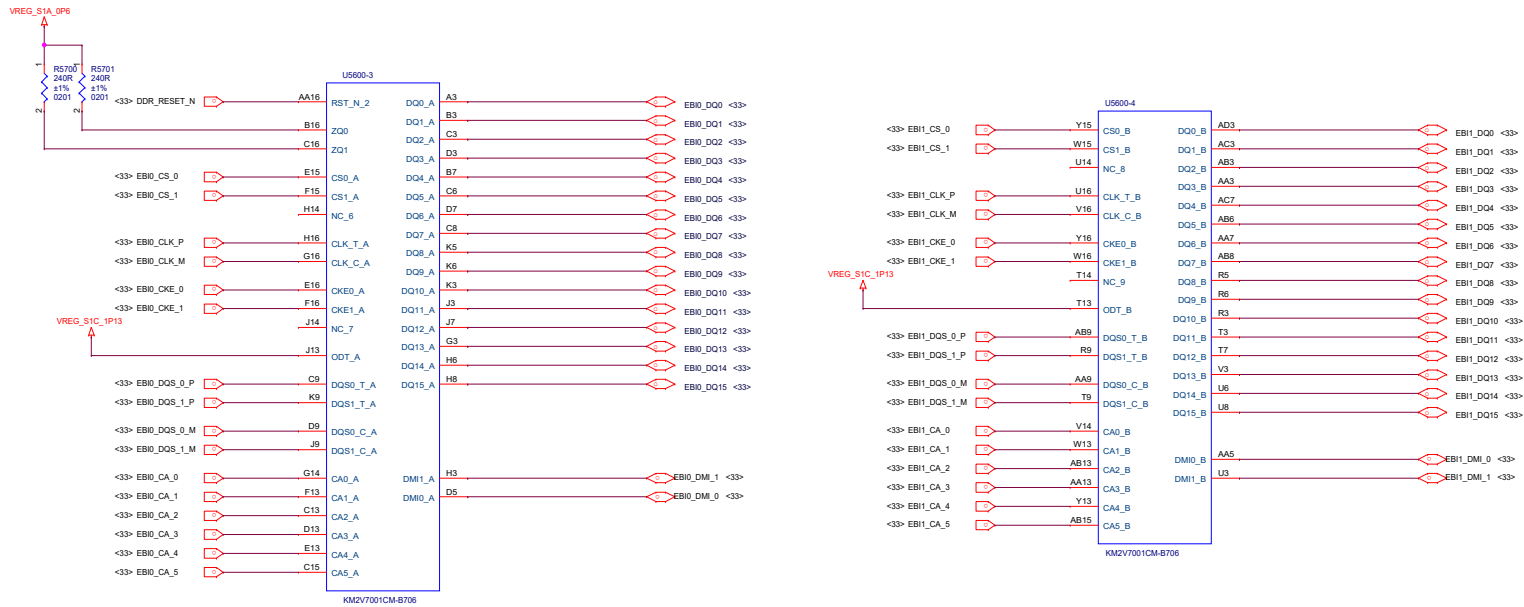








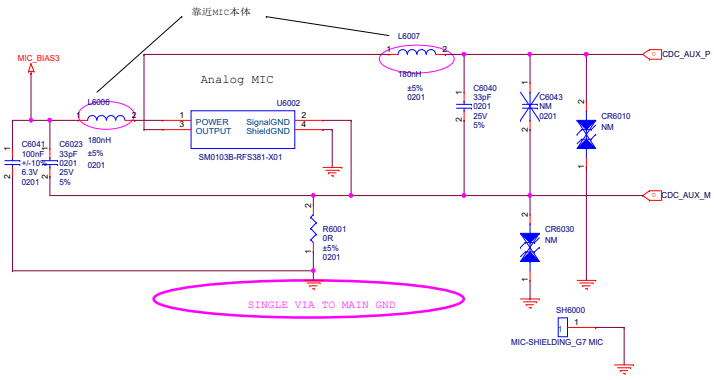
# LPDDR4 / 4x



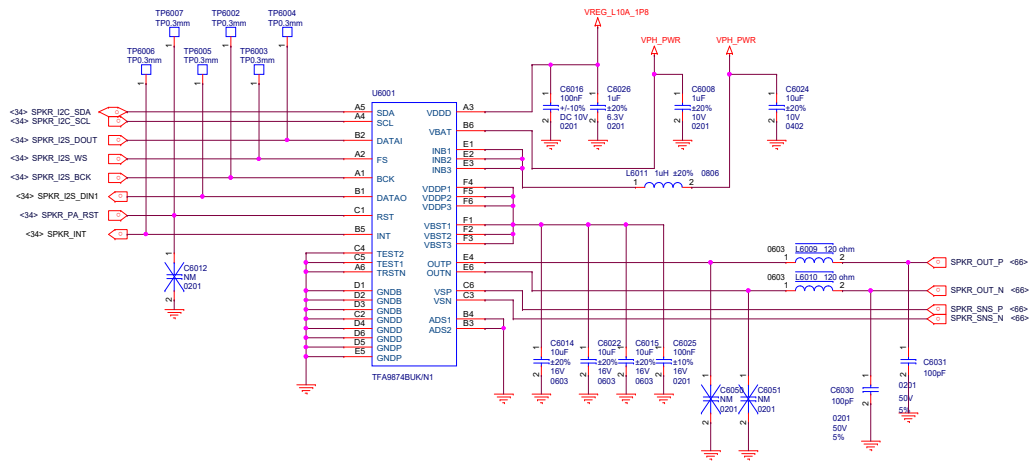




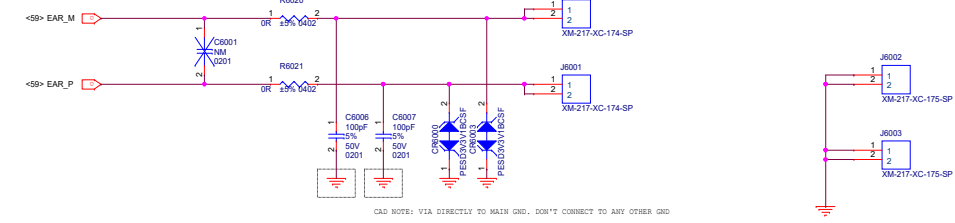
AUX MIC



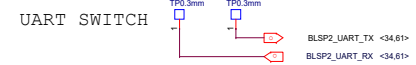
SPKR PA



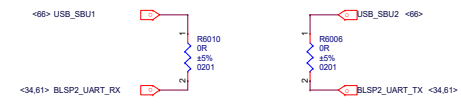
Receiver



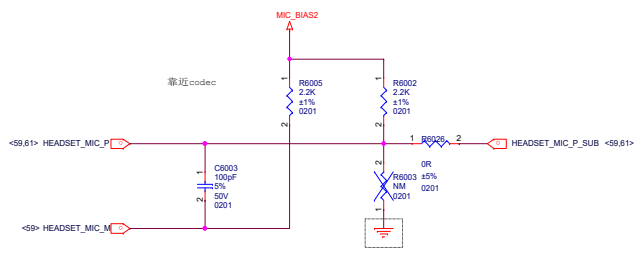
CAD NOTE: VIA DIRECTLY TO MAIN GND, DON'T CONNECT TO ANY OTHER GND



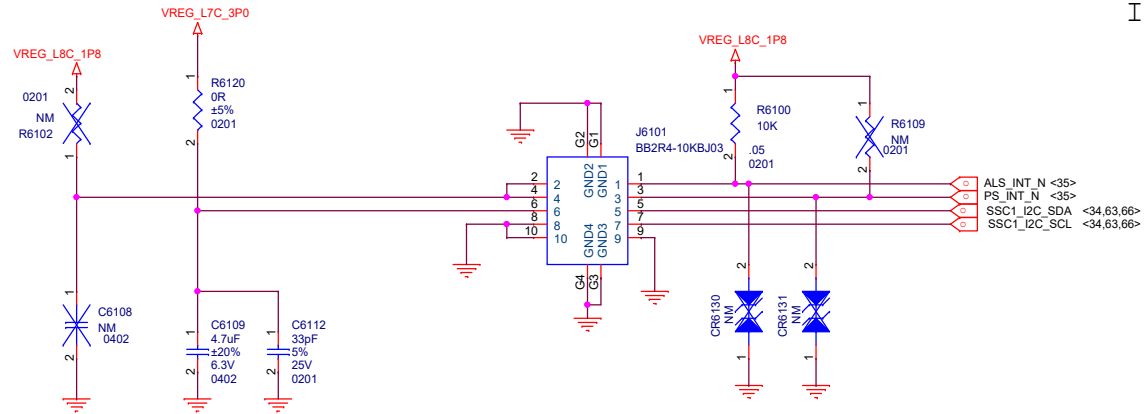
UART\_LOG/LPD



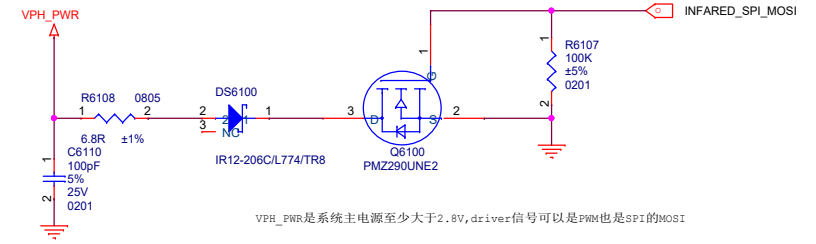
器件放到笼子外



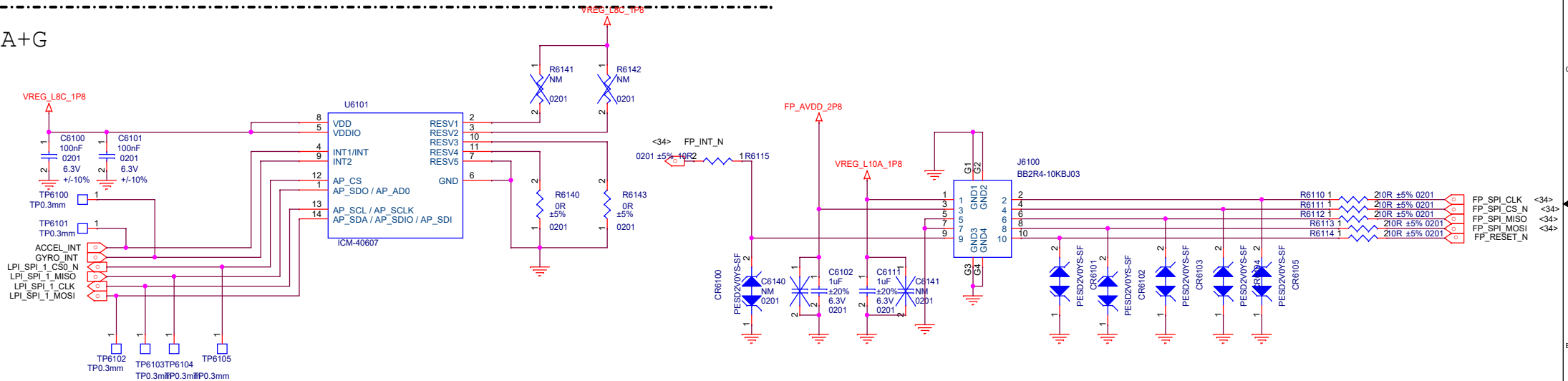
# L+P-sensor



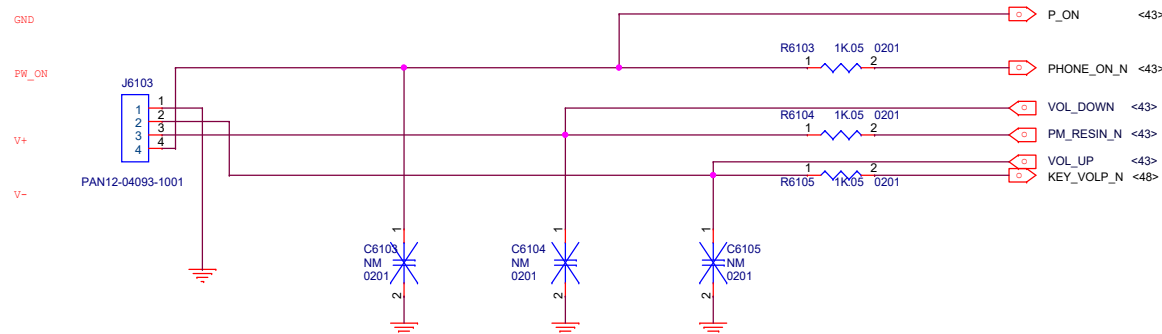
# INFARED



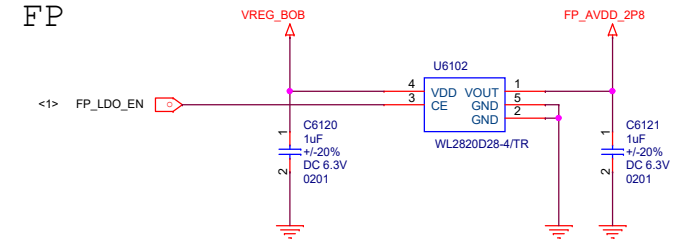
# A+G



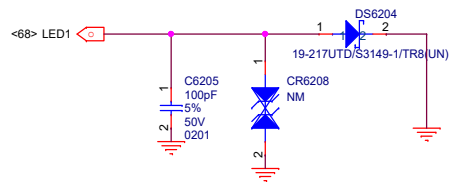
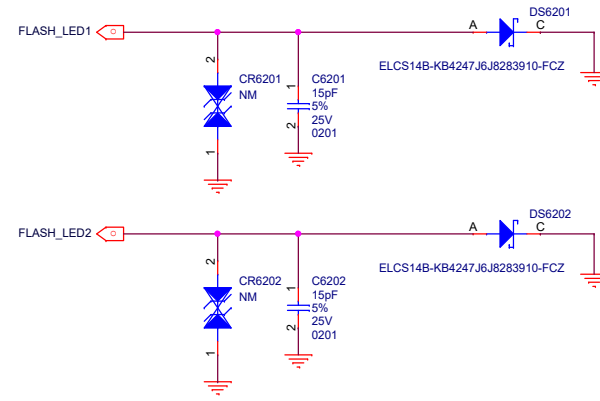
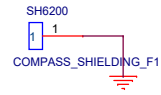
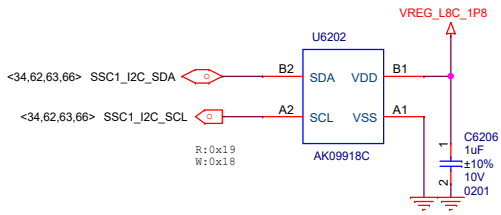
# Sidekey

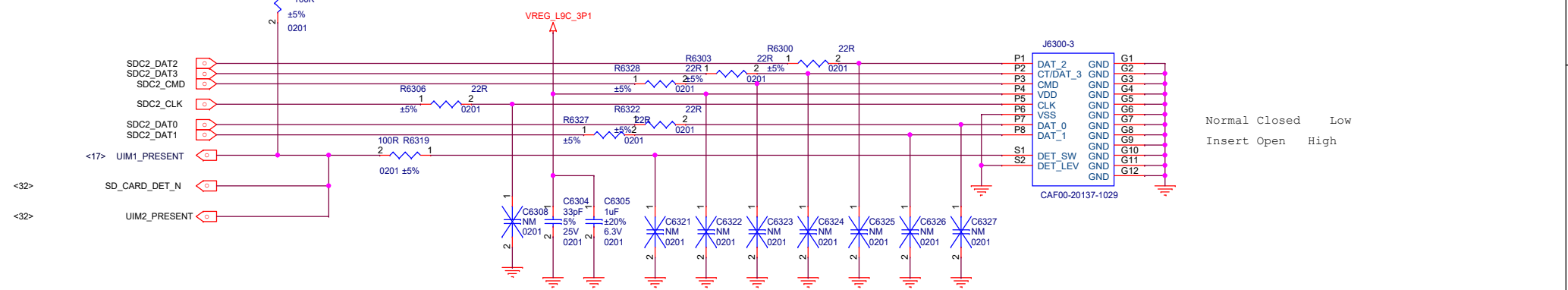
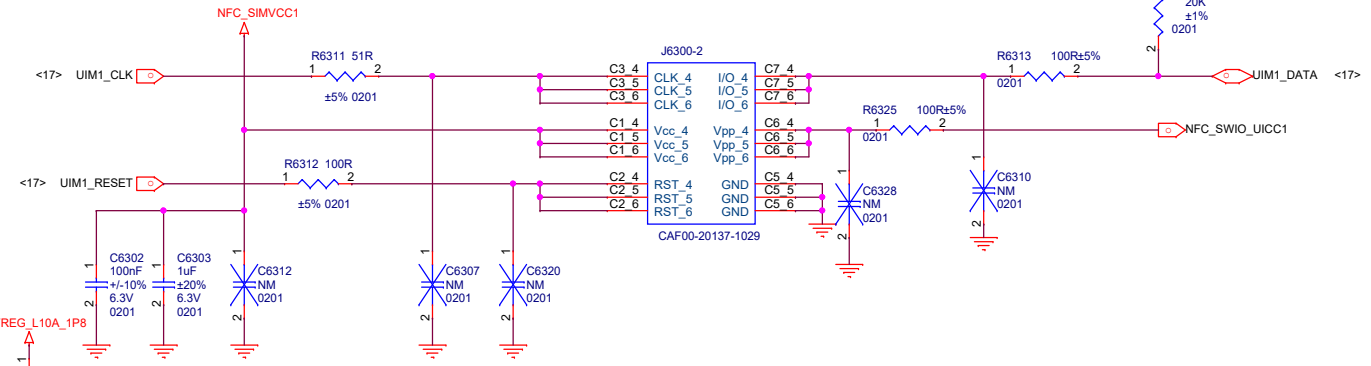
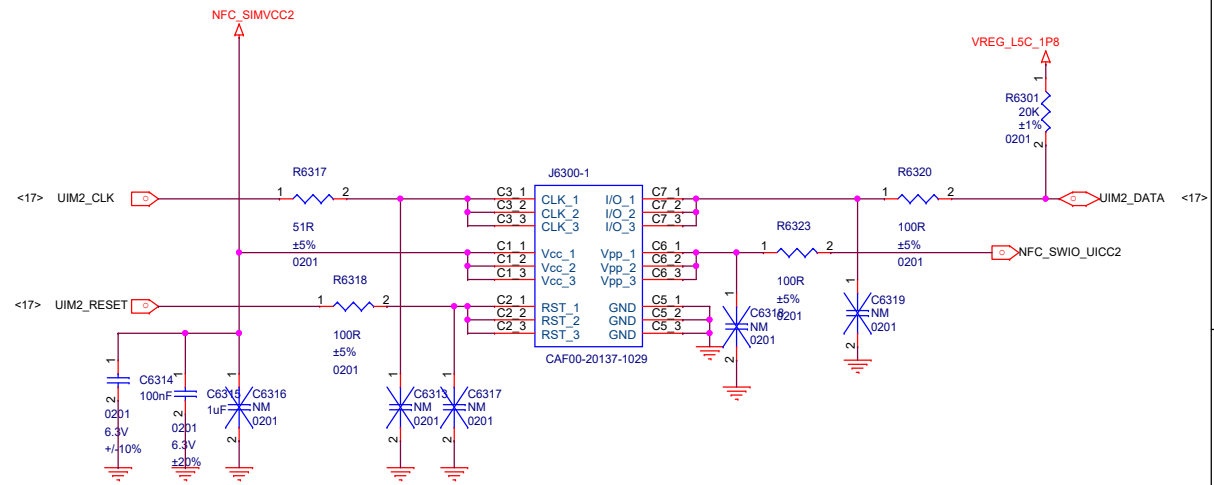


# FP



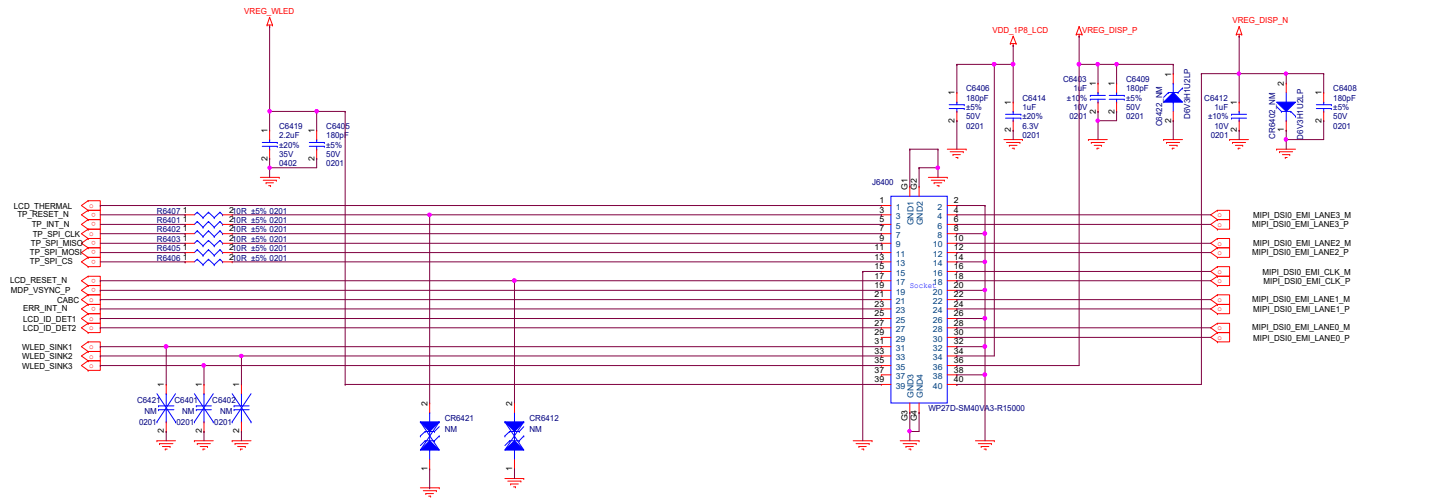
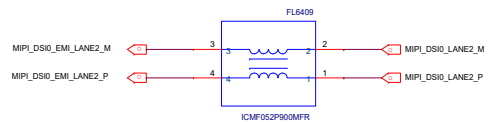
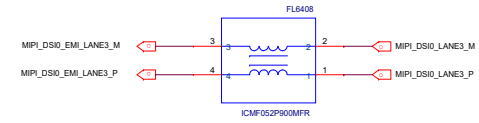
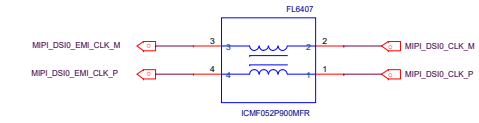
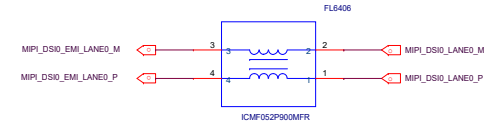
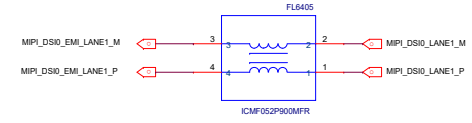
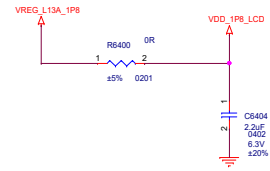
# COMPASS

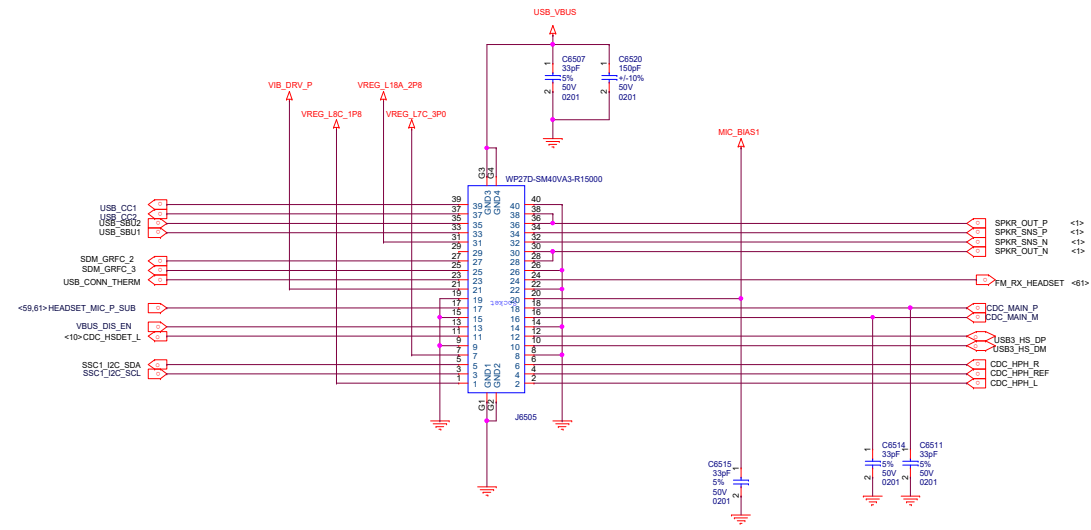
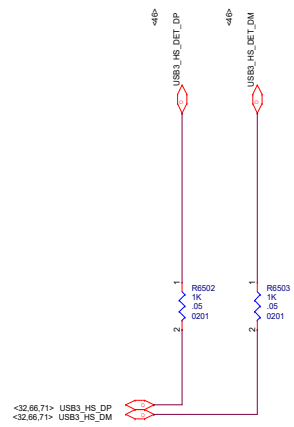




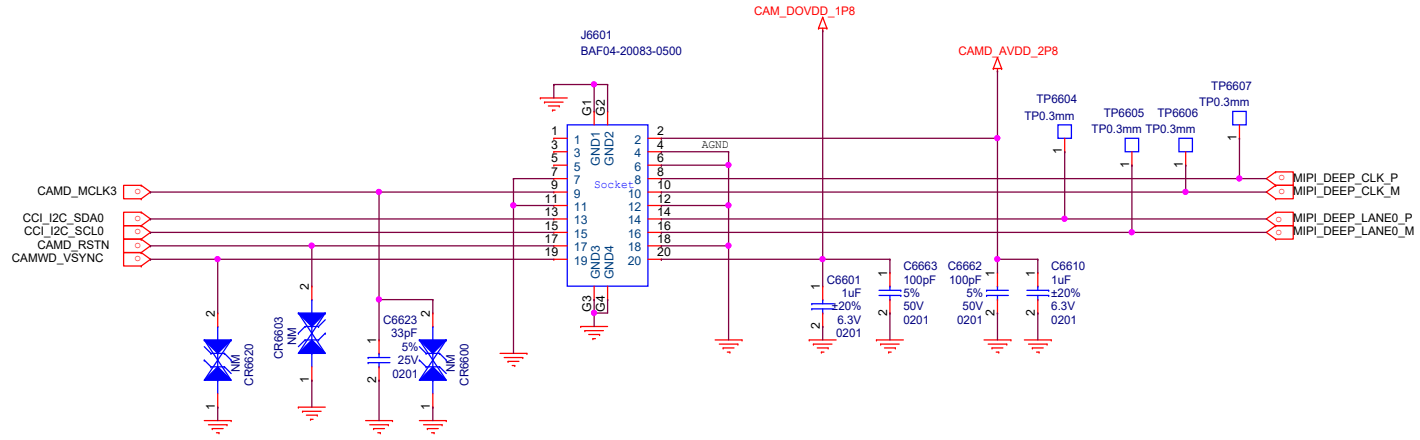
Normal Closed Low  
 Insert Open High



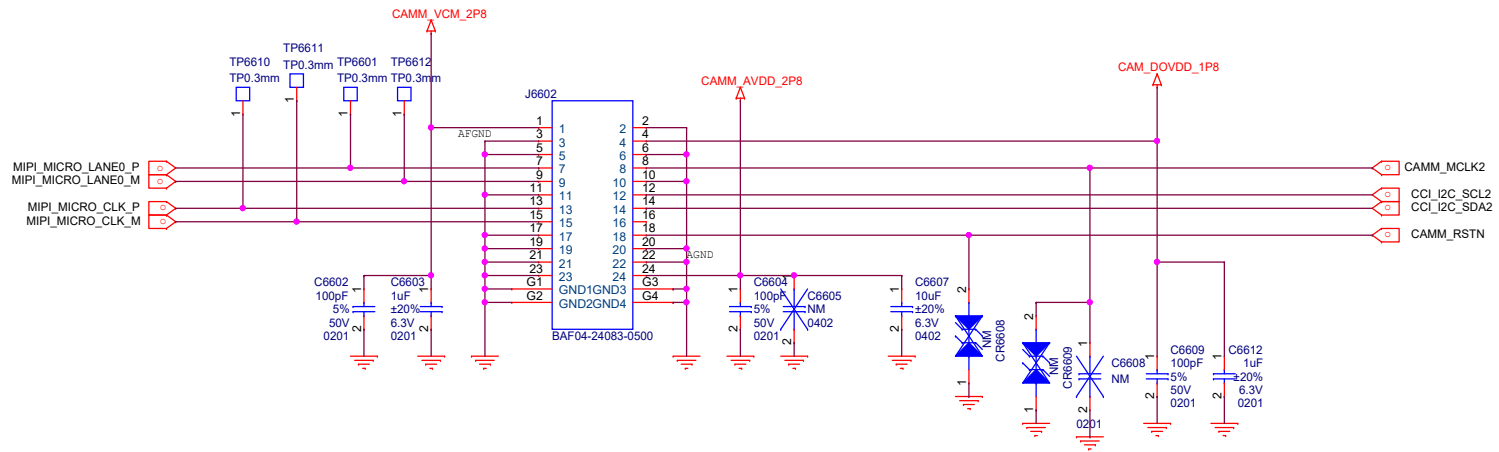




# 2M DEEP

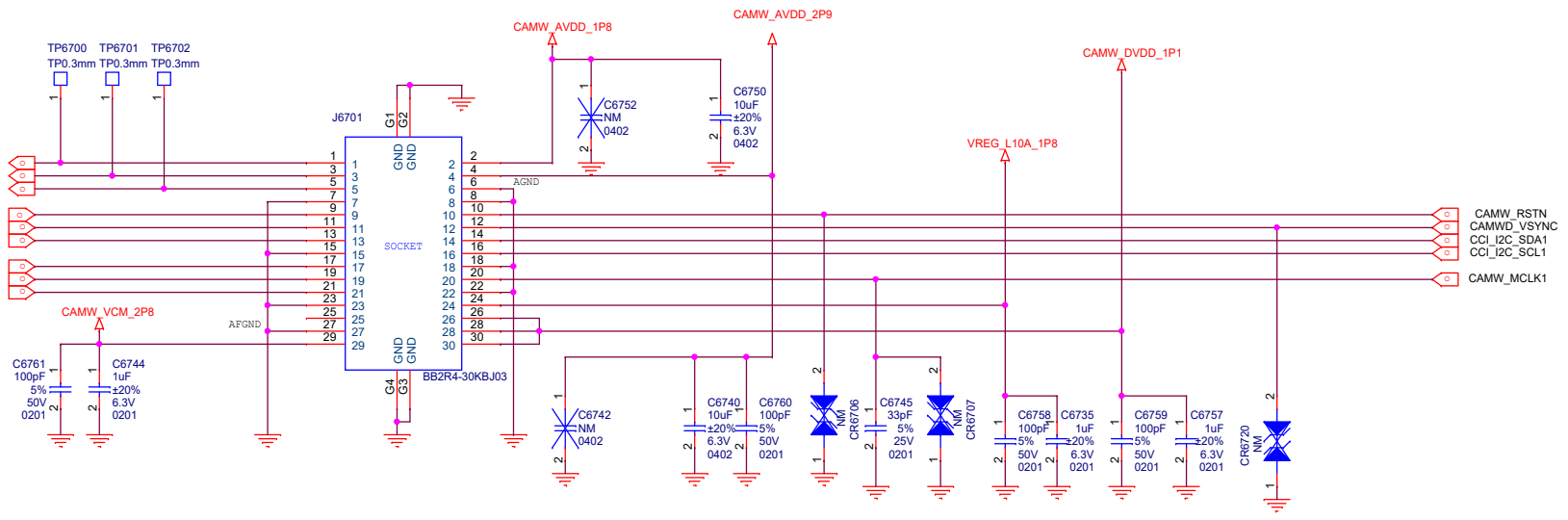


# 2M MICRO

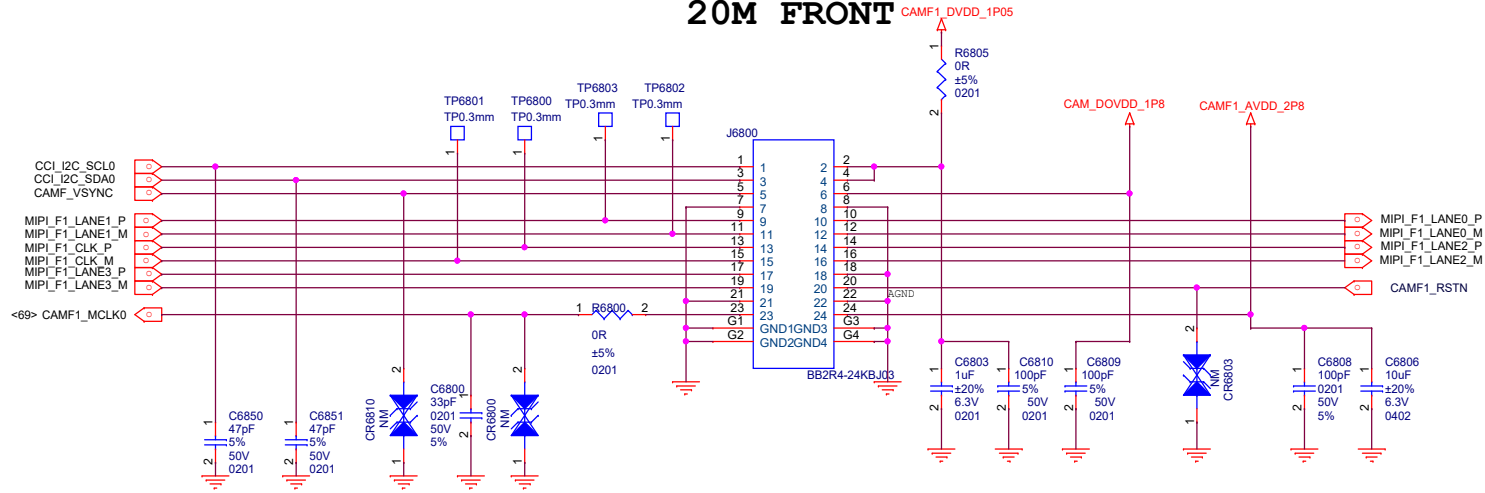


TP6700 TP6701 TP6702  
TP0.3mm TP0.3mm TP0.3mm

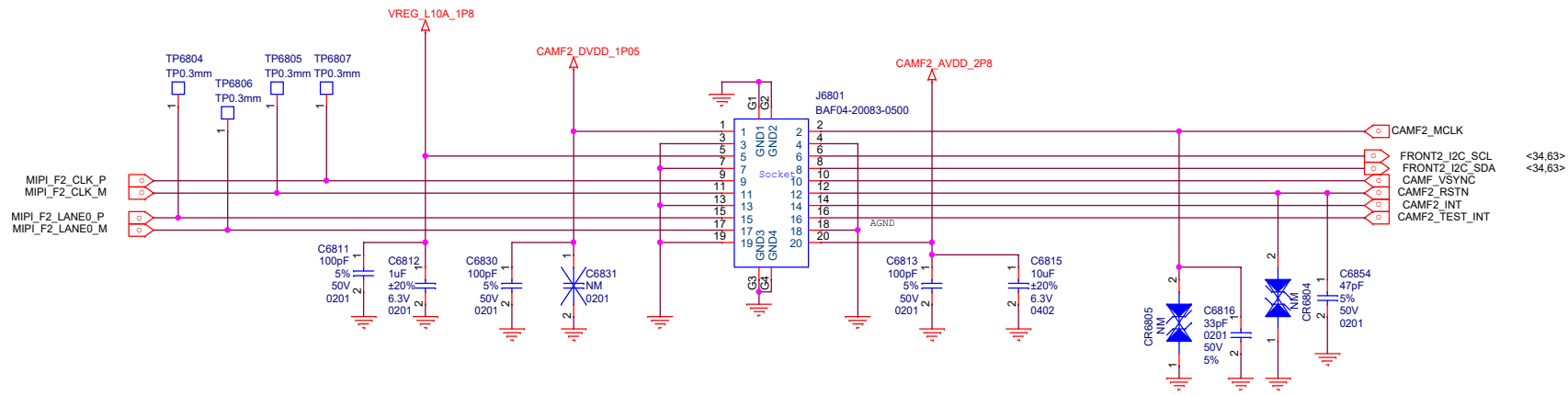
- <35> MIPI\_W\_trio0A
- <35> MIPI\_W\_trio0B
- <35> MIPI\_W\_trio0C
  
- <35> MIPI\_W\_trio1A
- <35> MIPI\_W\_trio1B
- <35> MIPI\_W\_trio1C
  
- <35> MIPI\_W\_trio2A
- <35> MIPI\_W\_trio2B
- <35> MIPI\_W\_trio2C

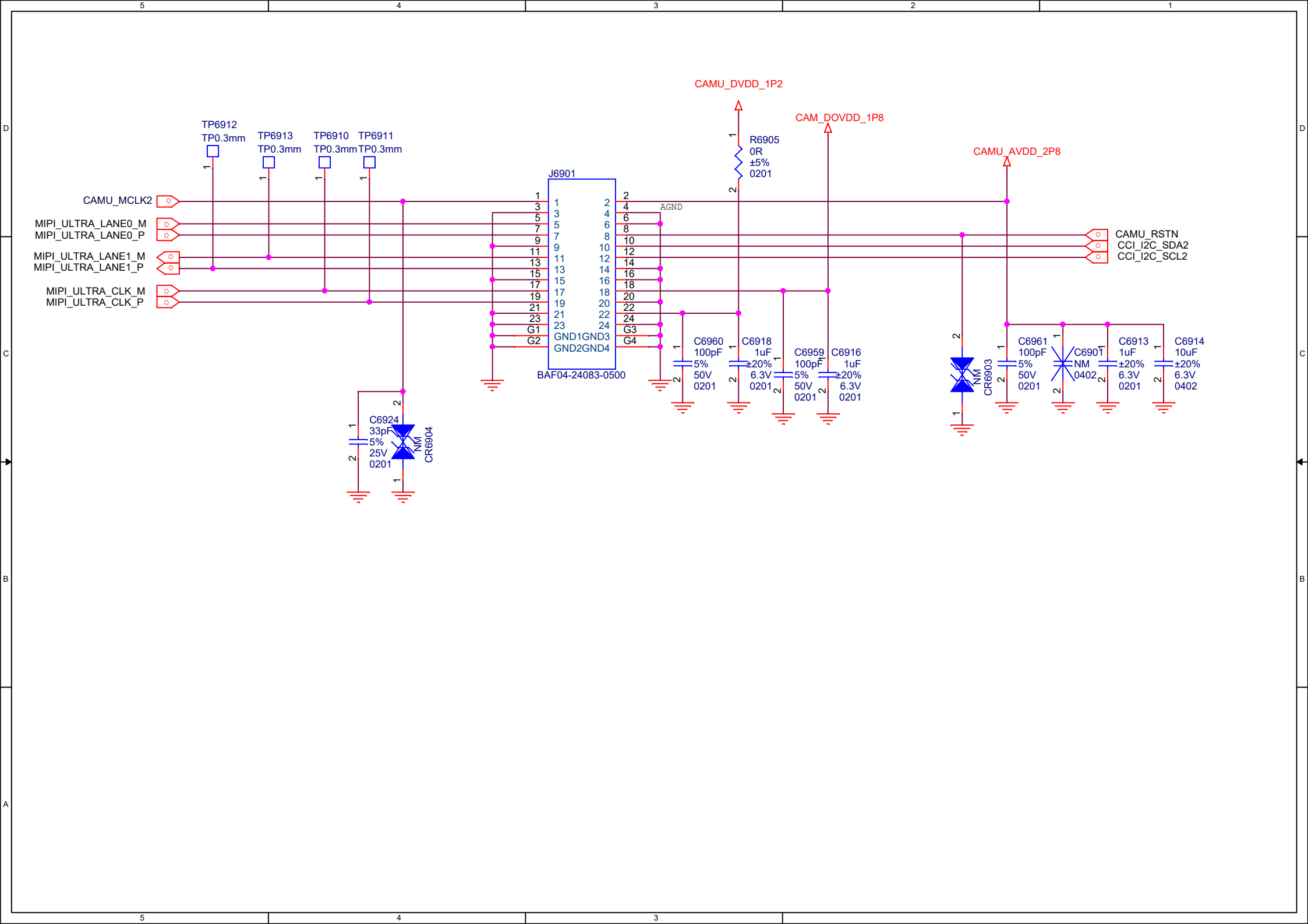


## 20M FRONT

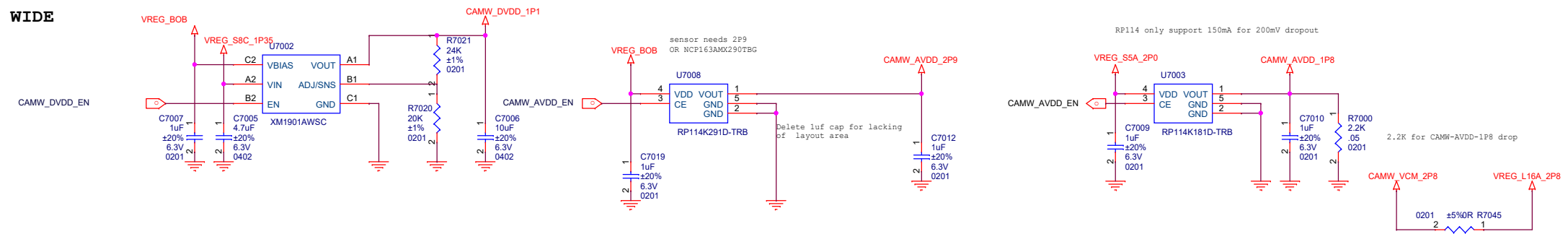


## 2M FRONT

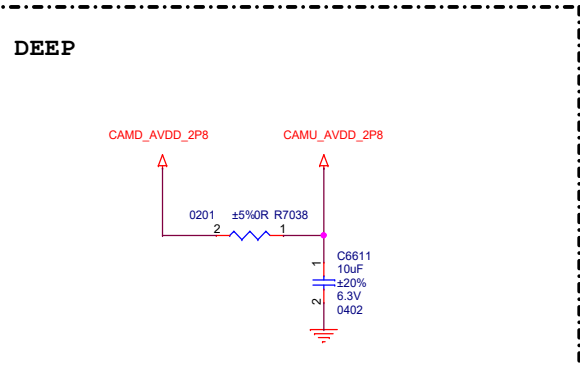




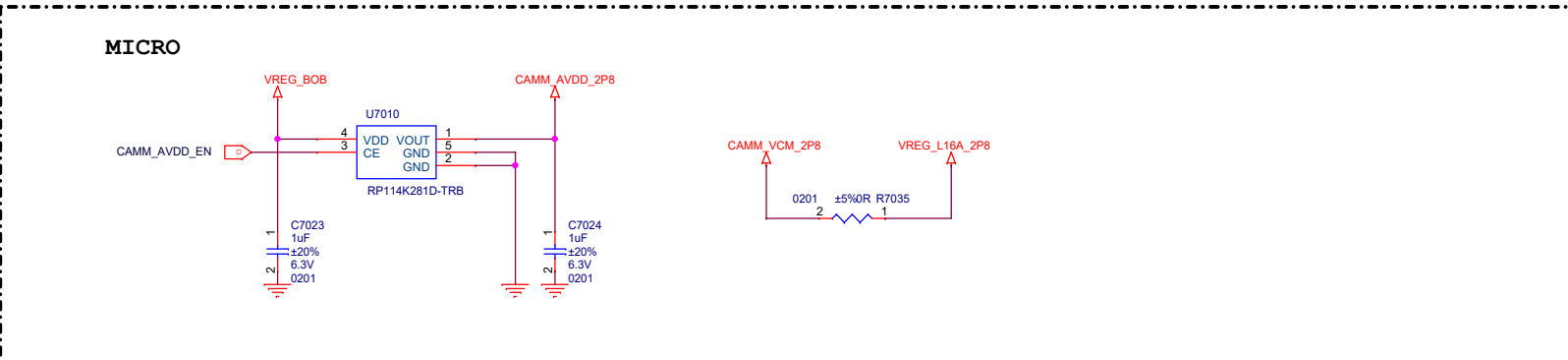
WIDE



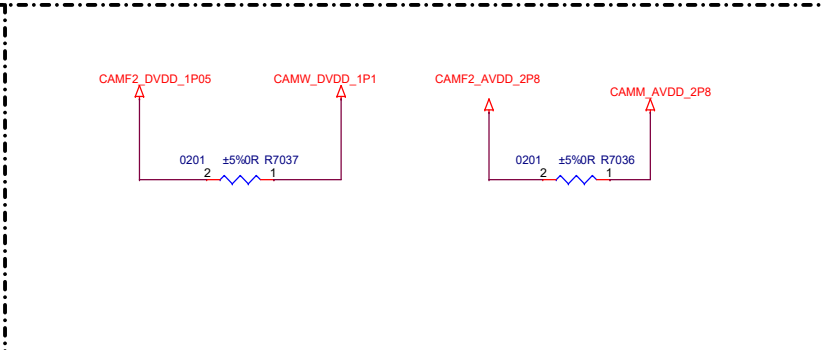
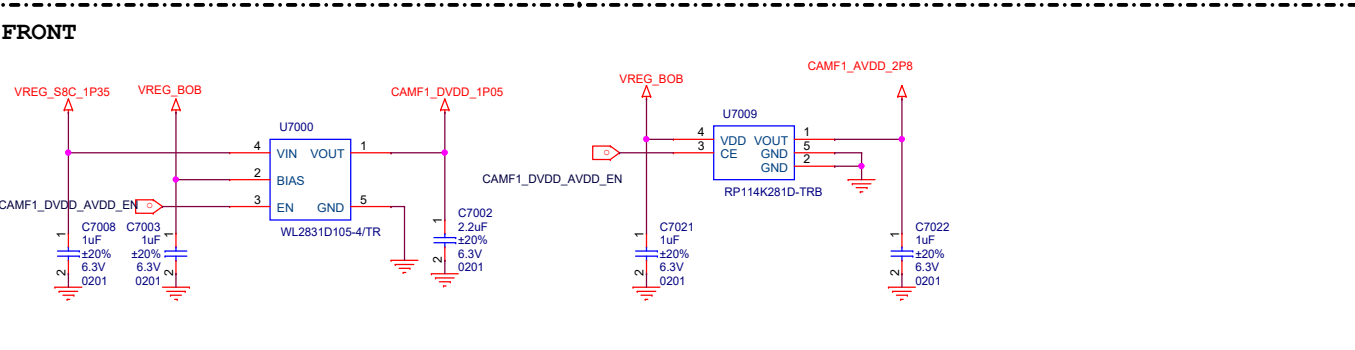
DEEP



MICRO



FRONT



ULTRA

